New Modeling Method and Design Optimization for a Soft-Switched DC–DC Converter

Liang Jia, *Member, IEEE*, Srikanth Lakshmikanthan, Xin Li, and Yan-Fei Liu, *Fellow, IEEE*

***Abstract*—High-performance cloud computing enables many key future technologies such as artificial intelligence (AI), self-driving vehicle, big data analysis, and the Internet of things (IoT), using clustered CPU and GPU servers in the datacenter. To improve the power efficiency and the infrastructure flexibility, the computing industry is adopting 54 VDC to power the servers in the open compute racks. In this paper, a new modeling technique for a soft-switched dc–dc converter is presented and suitable to guide optimal design in different applications, for example, 54 V to point of load (PoL) for the new open compute rack. To improve the model accuracy and reduce the complexity, this paper proposes a reduced-order linear differential equation (LDE) based modeling technique to discover the following: 1) the tank resonance involving the output inductor; 2) the output current ripple and its impact on power efficiency; 3) the proper on-time control for soft switching; 4) the unique bleeding mode under the heavy load; 5) the output power capability of the converter; and 6) component tolerance analysis and impact on the performance of the converter. With the power loss estimation, design guidelines are provided for a reference design and design improvement based on this new modeling technique. Using the proposed method, great accuracy can be expected in the efficiency estimation. Simulation and experimental results are provided to verify the modeling technique in a 54–1.2 V 25 A dc–dc converter prototype.**

***Index Terms*—Converter modeling, dc–dc converter, open compute project, soft switching.**

I. Introduction

ONE of the popular trends for powering high-performance datacenter is to supply the high-power-demanding workload servers with 54 VDC from the open compute racks [1]–[3], taking advantage of lower distribution losses and rack configuration flexibility. While the front-end stage of an ac–dc rectifier achieves power factor correction and regulates the bus voltage to a dc value on the rack busbar (54 V typical, the voltage range will be 40–60 V [1], considering regulation tolerance and battery backup mode), dc–dc step-down stage(s) will be required to further convert this bus voltage (and provide galvanic isolation, preferably) to point-of-load (PoL) voltage level, for example, 1 V.

Due to the large conversion ratio from 54 V-PoL (∼1 V), two-stage designs were conventionally and commonly used, where the first stage will convert 54 VDC from the rack to an intermediate bus voltage (often based on *LLC* resonant or pulsewidth-modulated (PWM) full-bridge converter [4]–[6]), for example, 12 VDC, and the second stage will be single or multiphase buck converter to power the PoL from the 12 VDC input [10]–[16]. The overall efficiency is limited by the multiplication of the efficiency of the two stages, especially at light load and maximum load [2], [17]. A new high-efficiency two-stage design was proposed in [7] and [8], where the first stage (PRM) regulates the intermediate bus with ZVS buck–boost converter, while the second stage (VTM) runs a fixed-ratio *LLC* resonant converter as a dc transformer. However, major drawbacks are the following: 1) no phase shedding for light-load efficiency; 2) no sinking capability for dynamic voltage identification (VID) down in CPU VR application due to the ZVS control of PRM; 3) not flexible for power scaling and roughly 100 W is the minimum power granularity available; and 4) nonisolated design (if isolation is preferred or required).

Recently, one-stage direct power conversion from 54 V-PoL attracts more and more interests to resolve the issues of the two-stage design. A wide range of isolated topologies is available for the high-conversion-ratio dc–dc application. First, *LLC* resonant converters could offer good efficiency; however, the input and output voltage variation might compromise the tank optimization and also the dynamic response is a big challenge with the conventional voltage mode control even with improved charge control [20]–[27].

Second, zero-voltage switching (ZVS) phase shift full bridge (PSFB) can be used in such applications and the current doubler configuration is suitable for high current output especially [28], [29]. Fig. 1 shows the PSFB converter schematic, switches A and B are switched complementary with 50% duty cycle minus a short dead time, and the same condition applies for switches C and D. The PWM signals for switches and key waveform of the converter are shown on the right side of Fig. 1. Phase shift control between the two switches pairs A, B and C, D is used for output voltage regulation. L_k is the total leakage inductance of the transformer plus external inductance if any to achieve ZVS in a certain load range [28], [29]. SR1 and SR2 are the synchronous rectification FETs. L1 and L2 are the output filter

Manuscript received April 9, 2017; revised July 4, 2017 and August 9, 2017; accepted September 2, 2017. Date of publication September 10, 2017; date of current version March 5, 2018. Recommended for publication by Associate Editor S. K. Mishra. *(Corresponding author: Liang Jia.)*

L. Jia and S. Lakshmikanthan are with the Consumer Hardware Engineering, Google Inc., Mountain View, CA 94043 USA (e-mail: liangjia@google.com; srikanthl@google.com).

X. Li is with Platforms, Google Inc., Mountain View, CA 94043 USA (e-mail: xinxli@google.com).

Y.-F. Liu is with the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON K7L 3Y4, Canada (e-mail: yanfei.liu@queensu.ca).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2751064

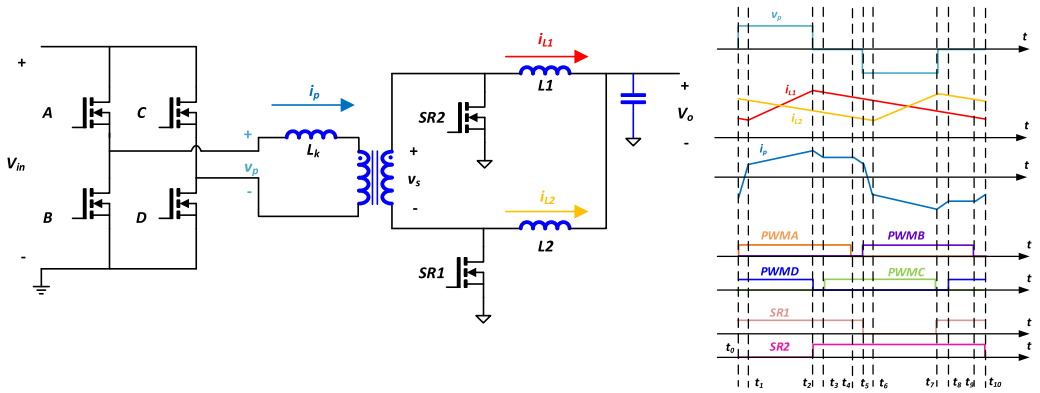

Fig. 1. PSFB converter schematic.

inductors to form the current double configuration. The output dc voltage is V_o.

There are a few limitations of ZVS-PSFB [28], [29].

A. Limited and Load-Dependent ZVS Range

In order to achieve ZVS on the primary side, leakage inductance L_k energy is required to fully charge/discharge the switching node of each of the legs before the switching on of the particular FET. Most of the time, switches C and D have more leakage energy due to the involvement of output inductor. But depending on the output load condition, the primary-side current i_p is varying, when switches A and B are turning on (at t_0 and t_4). Switches A and B may lose the ZVS turn on, especially at light load. So, in order to maximize the ZVS range at light load, the leakage energy has to be increased at all times, usually resulting in low conversion efficiency.

B. Secondary SR Driving

The reason of using SR to replace diode for high current application is to reduce the high conduction losses of the diode (caused by forward voltage V_f drop). However, the body diode of the FET is not designed for high switching/transient current. So, if the SR is not driven properly and forces the body diode to conduct current for an unnecessary period of time, the efficiency will suffer [28], [29]. The conventional gate drive signal for SR in PSFB converter discussed in [28] is duplicated from the primary-side gate drive signal (with some fixed propagation delay in gate signal transformer and gate driver), so the body diode is forced to conduct freewheeling current during the operation. The ideal SR driving signal is shown in Fig. 1 and some improved PSFB controllers (such as [30]) have dedicated control output signal to implement the proper SR driving to minimize the body diode conduction for better efficiency.

C. Reverse Recovery of SR

In PSFB current doubler converter, when the SR turns off, the freewheeling current will be forced to stop with a high *dv/dt*. Reverse recovery of the SR can be seen and losses will occur as well [31], [32]. In even worse situation for high voltage applications, if the *dv/dt* is too high, the induced current $I = C_{db}\frac{dv}{dt}$ or

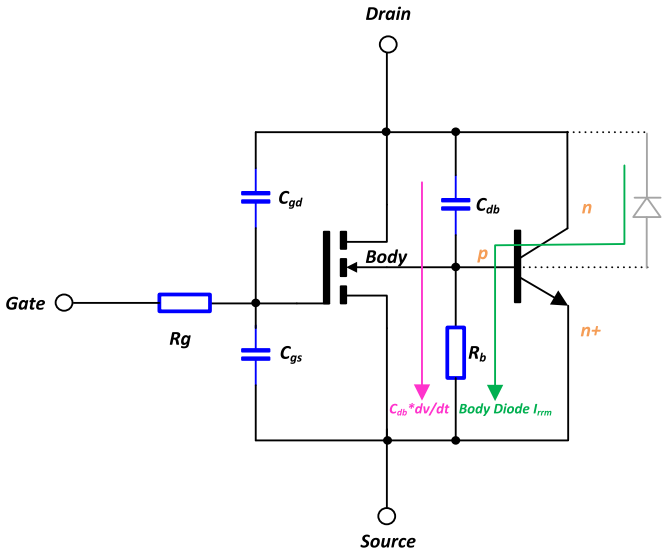

Fig. 2. MOSFET simplified structure.

the magnitude of the reverse recovery current passing through R_b is sufficiently large to cause injection across the $p-$ body $/n+$ source junction (in Fig. 2), the parasitic bipolar transistor may become active. This uncontrolled state of operation usually results in the destruction of the device.

Third, a half-bridge current doubler is proposed in [35] and a full-bridge current doubler is mentioned in [36] for 54 V-PoL application. The transformer is used for achieving high step-down ratio and isolation. However, the switches of these two topologies suffer from hard switching, resulting in higher switching losses and electromagnetic interference (EMI). So, the switching frequency of the topologies will be limited, as well as the power density, resulting in bigger size of the solution, nonideal placement on the motherboard and possibly higher power delivery losses. Another limitation for the implementation in [35] is that the output current capability cannot be scaled up by paralleling multiple cells to support higher current demanding payloads.

Also, nonisolated topologies are studied for 54 V-PoL direct conversion. For example, in [37] a synchronous buck converter using GaN FET is studied for a very high ratio step-down power

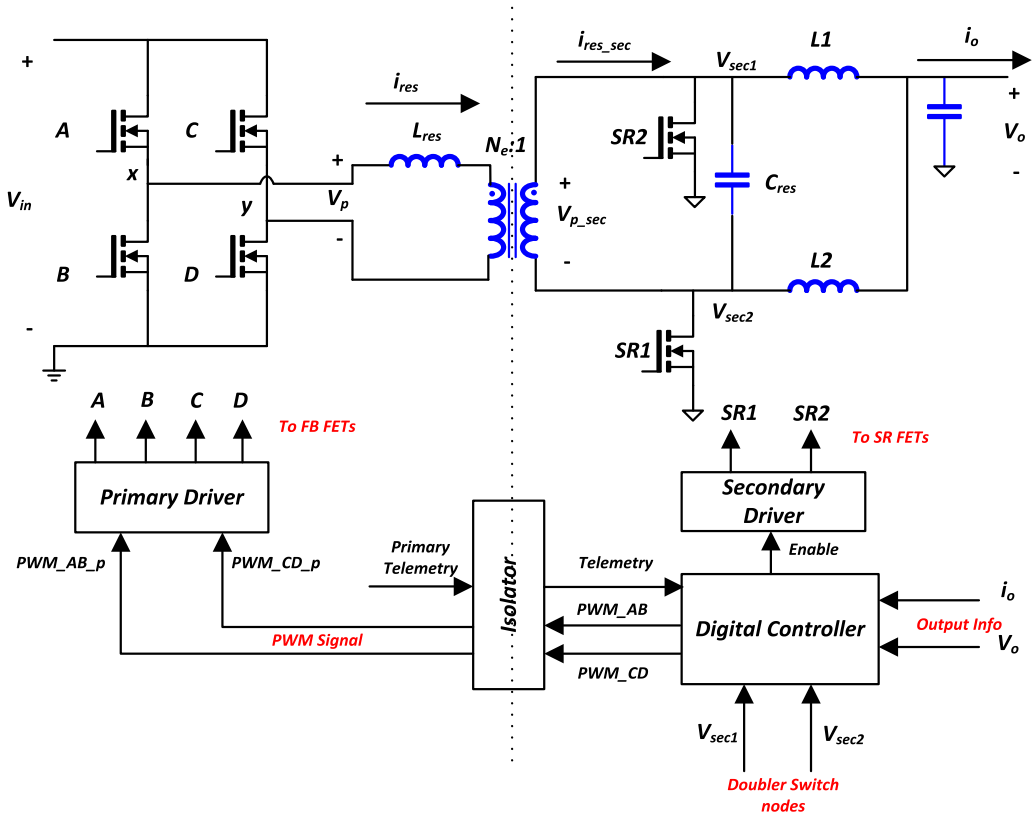

Fig. 3. System diagram with main controller and FET drivers.

conversion. Due to the super high switching speed of the GaN FET technology, the narrow duty cycle can be achieved. However, the efficiency is still lower compared with a transformer based Buck derived converter. Also, the dynamic performance will be very limited especially for unloading transient, because of the small duty cycle and high conversion ratio. In [38], a sigma converter concept was proposed with a fixed ratio converter and a regulated dc–dc converter (for example, buck converter) stacking up with each other. Ideally, the fixed ratio converter will process all the power efficiently without enabling the regulated converter. However, due to the input range is 40–60 V, the regulated converter will always process a fraction of the total power. Another concern for using the nonisolated converter in data center application is the grounding loop and current between multiple server trays. If an isolated topology can achieve similar or better efficiency, it will be highly preferred.

A new quasi-resonant (QR) PSFB converter with constant on-time (COT) control is studied in this paper and with the help of the secondary-side driver, the aforementioned limitations of the conventional PSFB are mitigated.

In this section, dc–dc converters for high down-conversion ratio are reviewed for datacenter application. And the brief review of the conventional phase shift full bridge converter will form the baseline for the future sections to demonstrate the advantages of the new topology with QR switching to achieve ZVS or ZVZCS for the primary and secondary switches for superior power efficiency.

This paper is organized as follows. In Section II, the operation principles are reviewed for the fundamental of the converter modeling. And due to the unique way of achieving secondary-side ZVZCS for the SR and COT control, light and heavy loading conditions are discussed separately. In Section III, the issue of the existing technique of modeling is outlined and limitations are highlighted. Equivalent circuits are built for different modes in the QR PSFB converter using the proposed method. Design examples are provided in Section IV using the proposed modeling technique for a reference design and a design improvement. In Section V, simulation and experimental results are demonstrated to verify the modeling. Finally, the conclusion will be drawn.

II. Principles of Operation of QR PSFB Current Doubler

In this section, the basic operations of quasi-resonant PSFB are discussed under light and heavy loading conditions. Unique modes are highlighted and compared with conventional PSFB. And this section provides the fundamental for the proposed modeling method in Section III.

A. QR PSFB Current Doubler System Implementation

In the system diagram shown in Fig. 3, the implementation is outlined. There are three chips within the controller scheme: primary full bridge gate driver, secondary-side SR gate driver

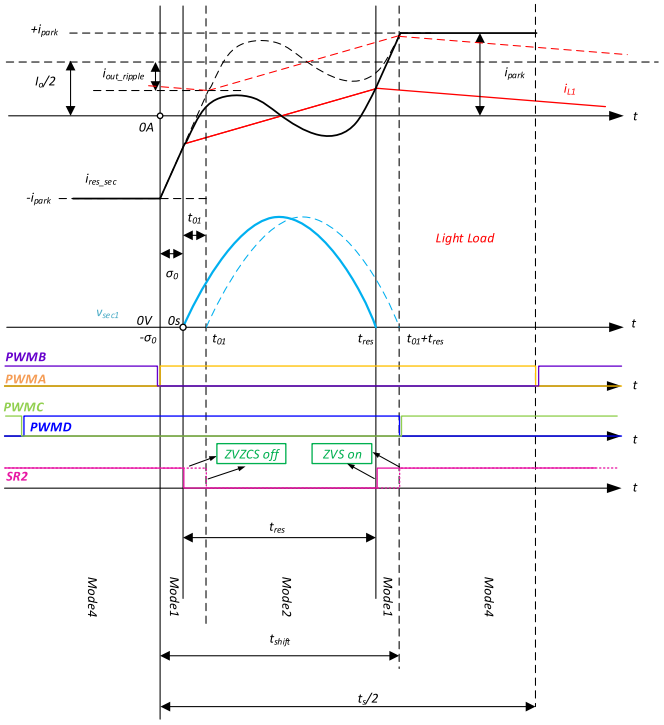

Fig. 4. Theoretical waveform for light load of QR-PSFB converter.

and the main digital controller. The controller is on the secondary side to improve the transient response performance and sends PWM signals PWM_AB and PWM_CD to primary-side driver via a digital isolator. And the primary-side driver outputs PWM_AB_p and PWM_CD_p to drive the FB. Telemetry information from the primary side will be sent back to the main controller via the digital isolator. The main digital controller also sends the Enable signal to the secondary-side gate driver to start detecting zero-current and zero-voltage events. Output current and voltage will be sensed directly on the secondary side. The control algorithm is COT control, and the switching frequency will be changed for output voltage regulation. The outstanding difference between this QR-PSFB and the conventional PSFB converter is the resonant capacitor C_{res} added on the secondary side.

B. Basic Operating Modes

In this section, basic modes are discussed for the QR-PSFB topology with COT control and ZVZCS detection using the secondary-side SR to highlight the advantages of the new converter. Different modes are defined based on the equivalent circuits and the same mode will have the same equivalent circuit. Key waveforms with timing definitions are shown in Figs. 4 and 10 under light-load and heavy-load conditions. Under light load, there will be two Mode 1 durations, while under heavy load, there is only one Mode 1 duration. For reference in both figures, the waveforms when $I_o = 0$ are shown in solid lines. In order to achieve ZVS on the primary side, the basic condition of $i_{\text{park}} > 0$ and $t_{\text{shift}} > t_{\text{res}}$ has to be met, where i_{park} is called the parking current when Mode 1 starts, t_{res} is the resonant period, and t_{shift} is the constant on time.

When the output has no loading, the time taken for $i_{\text{res\_sec}}$ to reach the i_{L1} level is defined as σ_0 in Fig. 4. In steady state, the positive and negative parking current $+i_{\text{park}}$ and $-i_{\text{park}}$ should have the same absolute value. And (1) is valid in steady state when $I_o = 0$

$$t_{\text{shift}} = 2\sigma_0 + t_{\text{res}} = 2\sigma_0 + \frac{2\pi}{\sqrt{\frac{L_{\text{res\_sec}}+L1}{L_{\text{res\_sec}}\cdot L1\cdot C_{\text{res}}}}}. \tag{1}$$

After applying a load to the output of the converter, it requires a longer time to ramp up $i_{\text{res\_sec}}$ to reach i_{L1} level in Fig. 4, and the additional time required is defined as t_{01}. t_{01} can be calculated by

$$t_{01} = \frac{I_o \cdot L_{\text{res}}}{2 \cdot N \cdot V_{\text{in}}}. \tag{2}$$

When $t_{01} > \sigma_0$ is met, we will have an additional operation mode-Mode 3 (i.e., bleeding mode), which only occurs during heavy loading shown in Fig. 10 between t_2 and t_3. The modes during different intervals are marked in Figs. 4 and 10 and the same mode has the same equivalent circuit and model, which will be discussed in Section III.

1) Light-Load Operation of QR-PSFB Converter ($t_{01} < \sigma_0$):

a) *Mode 1: $-\sigma_0 \le t < t_{01}$:* This mode (shown in Figs. 5 and 6) is very similar to PSFB converter, high-side FET of x phase FET A is turning on while low side FET B is turning off. The negative tank current i_{res} will discharge the equivalent output capacitance of the FET A before the FET A is turned on to achieve ZVS shown in Fig. 5. Secondary-side SRs are on still, so transformer voltage is clamped to nearly zero. And the primary-side current $i_{\text{res\_prim}}$ is rising with a slew rate of $V_{\text{in}}/L_{\text{res}}$ and the secondary-side current $i_{\text{res\_sec}}$ is rising with a slew rate of $N * V_{\text{in}}/L_{\text{res}}$.

b) *Mode 2: $t_{01} \le t < t_{01} + t_{\text{res}}$:* This is a unique mode for the new topology shown in Fig. 7. The current of the SR is sensed on the secondary side to determine the switching off moment. When the secondary-side tank current $i_{\text{res\_sec}} = i_{L1}$, the secondary-side driver will then turn off the SR FET SR2, so that zero-current switching (ZCS) off is achieved. And due to the added resonant capacitor C_{res}, the drain voltage V_{sec1} of SR2 will be rising with a very slow controlled slope, so ZVS is achieved at the same time. And the reverse recovery issue is addressed and the loss is mitigated. Now, the resonance happens in this mode. The sine shape voltage ($V_{\text{sec1}} - V_{\text{sec2}}$) across C_{res} is referred as the *bump voltage*. It is critical for the secondary-side driver controller to have very small time delay to detect the ZCS moment and turn off the SR. In a practical implementation, there might be some current flowing through the SR FET main channel before turn off, but due to the relatively high resonant capacitance C_{res} is added in the converter, the SR will not have any harmful high voltage spike or ringing at turn off (see Fig. 7).

c) *Mode 1: $t_{01} + t_{\text{res}} \le t < t_{\text{shift}} - \sigma_0$:* This mode has the same equivalent circuit as $-\sigma_0 \le t < t_{01}$ in Fig. 6. When the voltage across the SR2 V_{sec1} is resonating back to zero, the secondary-side driver will turn on SR2 to achieve ZVS on. And the primary-side FET A and D are still on, so the transformer voltage is clamped to nearly zero. And the primary-side current

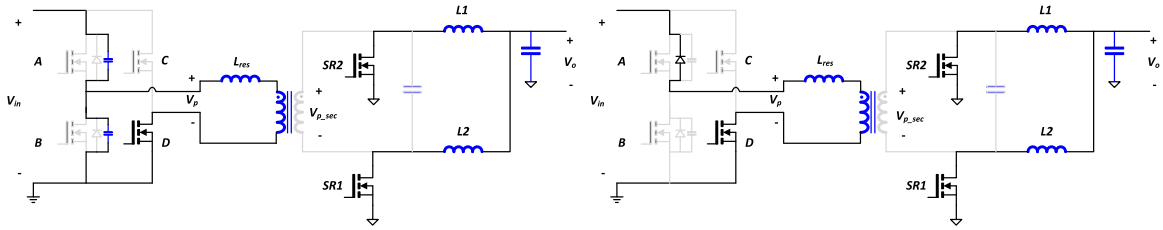

Fig. 5. ZVS on of FET A in Mode 1.

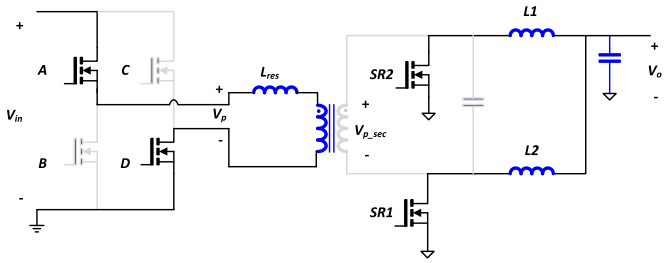

Fig. 6. Mode 1 of QR-PSFB converter.

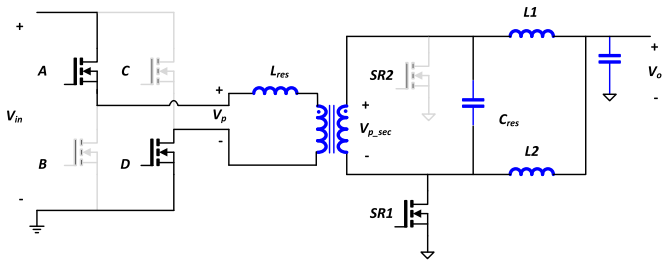

Fig. 7. Mode 2 of QR-PSFB converter.

$i_{\text{res\_prim}}$ is rising with a slew rate of $V_{\text{in}}/L_{\text{res}}$ and the secondary-side current $i_{\text{res\_sec}}$ is rising with a slew rate of $N * V_{\text{in}}/L_{\text{res}}$.

d) *Mode 4:* $t_{\text{shift}} - \sigma_0 \leq t < (t_s/2) - \sigma_0$*:* When the constant on time t_{shift} expires, the primary-side gate will turn off FET D and the positive parking current will discharge the equivalent output capacitance of FET C. After the equivalent output capacitor of FET C is fully discharged, the body diode will conduct as shown in Fig. 8. Then the FET C will be turned on with ZVS shown in Fig. 9. The parking current will remain nearly constant due to zero clamping voltage on the transformer. The positive i_{park} will help to achieve ZVS on for B FET later.

Due to the similarity of the switching transitions for the other half switching cycle, the details are omitted.

2) Heavy-Load Operation of QR-PSFB Converter ($t_{01} \geq \sigma_0$)*:* The theoretical waveform for heavy-load operation of the QR-PSFB converter is shown in Fig. 10 and the detailed modes of operation are discussed in this section.

a) Mode 1: $-\sigma_H \leq t < t_{01}$*:* This mode is the same as light-load condition and the FET A is turned on with ZVS and the current $i_{\text{res\_sec}}$ is ramping up to catch i_{L1}. To differentiate the time interval of σ_0 in the steady state under light load and when $I_o = 0$, the time taken for $i_{\text{res\_sec}}$ to reach $-i_{\text{out\_ripple}}$ from $-i_{\text{park}}$ is defined as σ_H for heavy-load condition.

b) Mode 2: $t_{01} \leq t < t_2$*:* This mode is the same as light-load condition at the beginning, when the secondary-side tank current $i_{\text{res\_sec}} = i_{L1}$, the secondary-side driver will turn off the SR FET SR2, so that ZVZCS off is achieved. However, in heavy-load condition, the full resonance will not finish due to constant on time control scheme. So at t_2, the primary-side driver will switch off FET D, due to the expiration of t_{shift}. And the time t_2 can be calculated by

$$t_2 = t_{\text{shift}} - \sigma_H = t_{\text{shift}} - \frac{\left(i_{\text{park}} - i_{\text{out\_ripple}}\right) \cdot L_{\text{res}}}{N \cdot V_{\text{in}}}. \quad (3)$$

c) Mode 3: $t_2 \leq t < t_3$*:* This mode is unique in heavy load, and at t_2, the equivalent circuit is shown in Fig. 11. The positive i_{park} discharges the output capacitance of FET C until the body diode conducts.

Then the FET C will be turned on with ZVS shown in Fig. 12. Different from Mode 4, the SR2 in this mode is off. And in this mode, the tank of L_{res} and C_{res} are discharging to support the output load. The secondary-side driver will turn on SR2, when V_{sec1} is discharged to zero to achieve ZVS on.

d) Mode 4: $t_3 \leq t < (t_s/2) - \sigma_H$*:* At t_3, SR2 is turned on and then this mode is the same as light-load condition shown in Fig. 9. The parking current will remain nearly constant due to zero clamping voltage on the transformer. The positive $+i_{\text{park}}$ will help to achieve ZVS on for B FET later.

Due to the similarity of the switching behavior for the other half switching cycle, the details are omitted for simplicity.

III. Modeling of a QR-PSFB Converter

Although simulation tools can always be used for simulating the switching converters in a much easier way, the circuit parameters remain in nonclosed form, and it is difficult to tell the impact of a certain design parameter on the results. Also, experiments often take time and additional delay will be expected if magnetics changes are needed. On the other hand, a mathematical model can give us very intuitive information, which can always help the designer to do the following: 1) fully understand the operation of the switching states; 2) reduce the number of iterations for optimization in experiments; 3) find worst case/corner case for testing; and 4) analyze component tolerance impacts.

In [19], the paper discussed the modeling of a very similar 48 V VR converter using second order differential equations, if the output filter inductance is much larger than the resonant inductance. So the output load is modeled as a constant current source and the output inductor is not participating resonance.

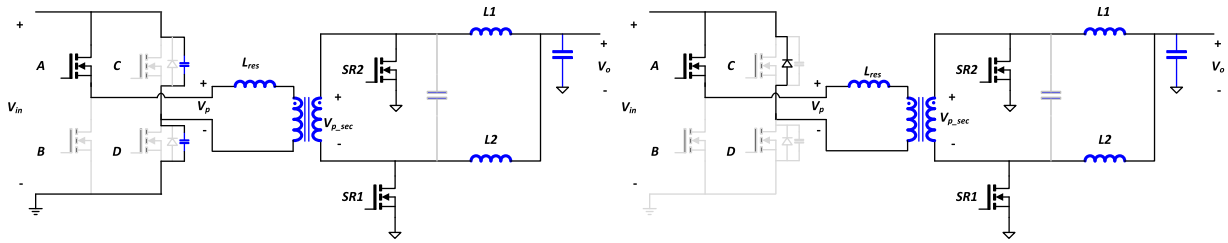

Fig. 8. ZVS on of FET C in Mode 4.

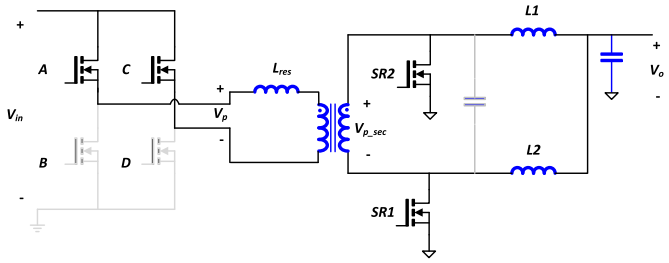

Fig. 9. Mode 4 of QR-PSFB converter.

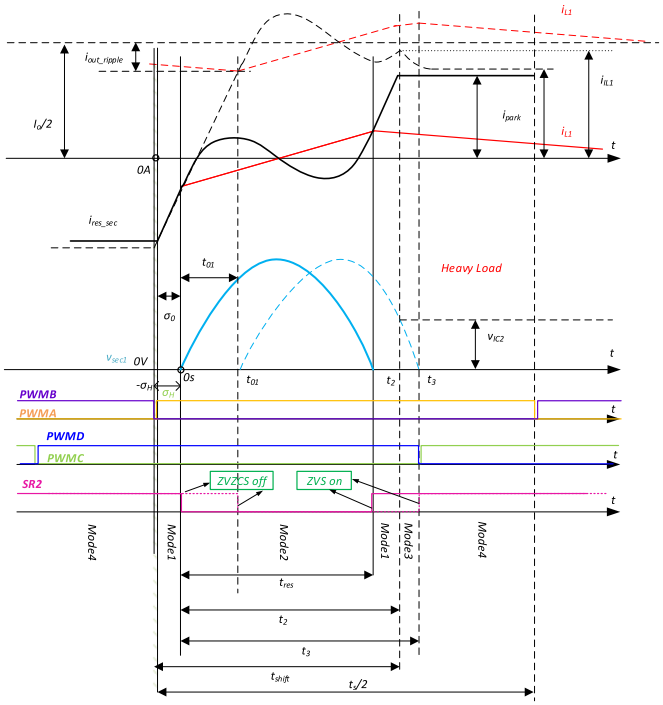

Fig. 10. Theoretical waveform for heavy load of QR-PSFB converter.

However, the accuracy is not quite good to match simulation and experiments in low voltage high current PoL voltage regulator (VR) application. In PoL VR application, the output inductor is usually small to improve transient performance, even though it will suffer from bigger output current ripple and root-mean-square (rms) losses [12]. The large current ripple will be filtered by output capacitor banks, which is usually in millifarad range, to have very low output voltage ripple (for example, 1% of V_o). So in this paper, a *new* modeling method is proposed to improve the accuracy of the model, which now includes the output inductor into tank resonance and considers the output current ripple for losses estimation. Due to the relatively big output capacitance, the load can be modeled as a dc voltage source and a load resistor. Compared with a fourth-order complete (*LCLC*) model, this new reduced-order model is less complicated but offers very similar accuracy.

Assumptions:

1) transformer is ideal and lossless;
2) dead time in the FB and its impact is negligible;
3) inductors and capacitors are ideal, no DCR or ESR, etc.;
4) V_s (the reflected voltage of V_p on the secondary side) is an ideal source and all the solid-state switches are ideal;
5) output voltage ripple is negligible;
6) the equivalent model is reflected to the secondary side.

So, the secondary-side input voltage V_s can be modeled as a dc source or a short circuit, depending on the operation modes. C_{res} is the resonant capacitor. $L_{\text{res\_sec}}$ is the reflected leakage inductor on the secondary side, where $L_{\text{res\_sec}} = \frac{L_{\text{res}}}{N_e{}^2}$. N_e is the turns ratio of the transformer. $L1$ is the output inductor per phase. Due to the high output capacitance, the output is modeled as DC source and $<1\%$ output voltage ripple is ignored, resulting in negligible modeling error but significantly reduced complexity.

A. Mode 1: Duty Cycle Loss Mode

The duty cycle loss mode of QR-PSFB is the same as the conventional PSFB converter in Fig. 13, where the input voltage V_s is applied to the resonant inductor $L_{\text{res\_sec}}$. State equations can be written as

$$\begin{cases} V_{L\text{res\_sec}} = V_s = \frac{V_{\text{in}}}{N_e} = L_{\text{res\_sec}} \cdot \frac{d}{dt} i_{\text{res\_sec}}(t) \\ V_{L1} = -V_o = L1 \cdot \frac{d}{dt} i_{L1}(t) \end{cases}. \tag{4}$$

B. Mode 2: Power Delivery Mode

The SR on the secondary side is released, when $i_{\text{res\_sec}} = i_{L1}$ and resonance between $L_{\text{res\_sec}}$, L_1 and C_{res} happens (in Fig. 14). State equations can be written in (5) and the initial condition can be calculated in (6) (see Fig. 14)

$$\begin{cases} V_s = \frac{V_{\text{in}}}{N_e} = v_{L\text{res\_sec}}(t) + v_{C\text{res}}(t) \\ v_{C\text{res}}(t) = v_{L1}(t) + V_o \\ i_{C\text{res}}(t) = i_{\text{res\_sec}}(t) - i_{L1}(t) \end{cases} \tag{5}$$

$$\begin{cases} v_{C\text{res}0} = 0 \\ i_{\text{res\_sec}0} = \frac{1}{2} I_o - i_{\text{out\_ripple}} \end{cases}. \tag{6}$$

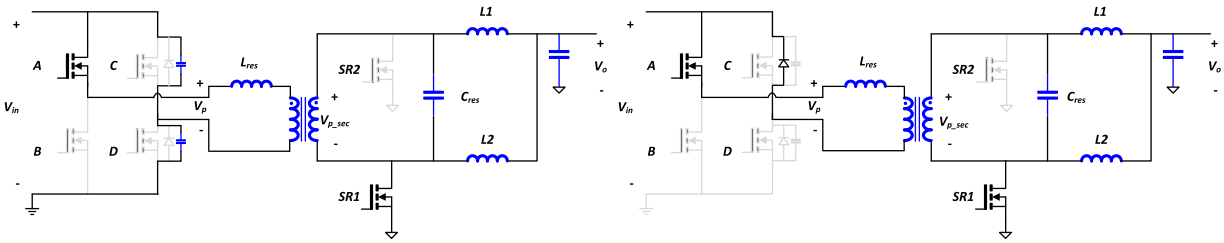

Fig. 11. ZVS on of FET C in Mode 3.

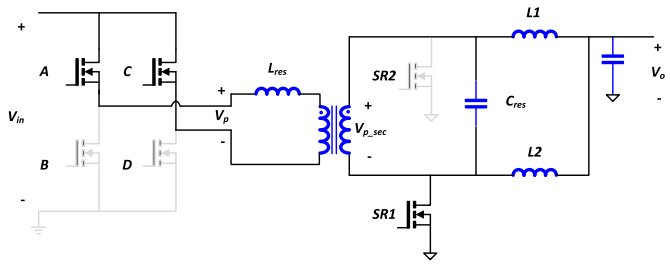

Fig. 12. Bleeding mode of QR-PSFB converter.

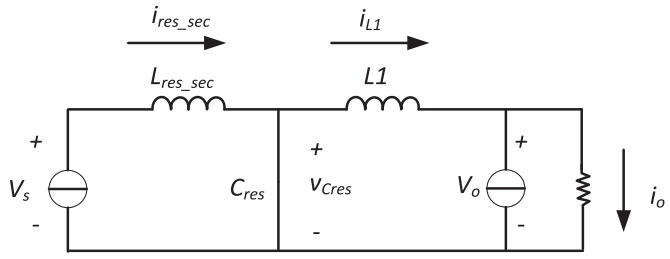

Fig. 13. Mode 1 equivalent circuit of the proposed model.

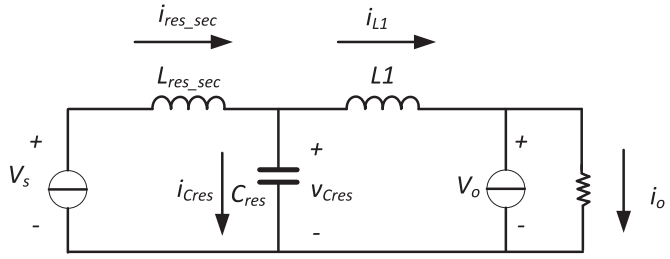

Fig. 14. Mode 2 equivalent circuit of the proposed model.

C. Mode 3: Bleeding Mode

The bleeding mode is another unique mode of this new topology shown in Fig. 15. Due to the ZVZCS feature of secondary-side SR control and driving, when the primary-side x or y phase both upper (FET A and C) or lower FETs (FET B and D) are on, the input of the model is a short circuit, while SR is still off. So this mode is called bleeding mode, since $L_{\text{res\_sec}}$ and C_{res} are now discharging to the load together. State equations are as follows in (7), where V_{IC2} and i_{IL1} are the initial conditions of

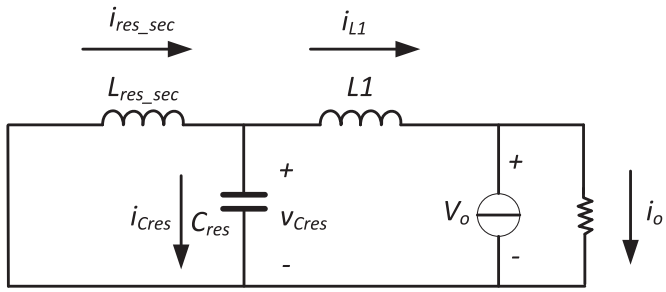

Fig. 15. Mode 3 equivalent circuit of the proposed model.

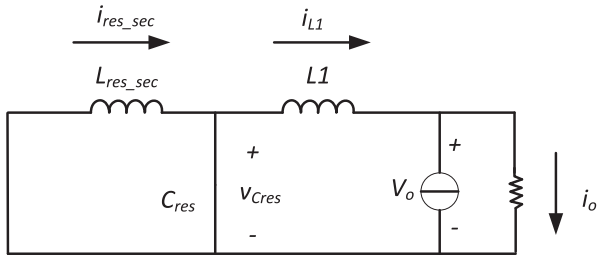

Fig. 16. Mode 4 equivalent circuit of the proposed model.

the resonant capacitor voltage $v_{C\text{res}}$ and inductor current $i_{L\text{res\_sec}}$ at time t_2 shown in Fig. 10 and expressed in (8)

$$\begin{cases} v_{L\text{res\_sec}}(t) + v_{C\text{res}}(t) = 0 \\ v_{C\text{res}}(t) = v_{L1}(t) + V_o \\ i_{C\text{res}}(t) = i_{\text{res\_sec}}(t) - i_{L1}(t) \end{cases} \tag{7}$$

$$\begin{cases} v_{C\text{res}0} = V_{IC2} = v_{\text{sec}1}(t_2) \\ i_{\text{res\_sec}0} = i_{IL1} = i_{\text{res\_sec}}(t_2) \end{cases}. \tag{8}$$

D. Mode 4: Freewheeling Mode

When $V_{\text{sec}1} = 0$ or $V_{\text{sec}2} = 0$, the secondary-side driver will turn on the SR, so C_{res} is shorted. And $i_{\text{res\_sec}}$ will remain constant and output inductor current is freewheeling through SRs (in Fig. 16). State equations can be written as

$$\begin{cases} V_{L\text{res\_sec}} = L_{\text{res\_sec}} \cdot \frac{d}{dt} i_{\text{res\_sec}}(t) = 0 \\ V_{L1} = -V_o = L1 \cdot \frac{d}{dt} i_{L1}(t) \end{cases}. \tag{9}$$

E. Solutions of the State Equations

In order to present the system in a closed form, the third-order differential equations (4)–(9) have to be solved for each of the modes. The final value of the previous state will be substituted into the next state for initial condition.

In Mode 1, the current $i_{\text{res\_sec}}(t)$ will ramp up to $i_{L1}(t)$ level linearly. Then we will enter the Mode 2. The equations for $i_{\text{res\_sec}}(t)$ and $v_{C\text{res}}(t)$ can be expressed in (11) and (12), where the equivalent resonant frequency is shown in (10). It is worth mentioning that the inductance L1 is involved in the resonance, which is ignored in the model proposed in [19]

$$\omega_{\text{res}} = \sqrt{\frac{L_{\text{res\_sec}} + L1}{L_{\text{res\_sec}} \cdot L1 \cdot C_{\text{res}}}} \tag{10}$$

$$\begin{aligned} i_{\text{res\_sec}}(t) = {} & \frac{I_{\text{out}}}{2} + \frac{\frac{V_s}{L_{\text{res\_sec}}} - \frac{V_s - V_o}{L_{\text{res\_sec}} + L1}}{\omega_{\text{res}}} \cdot \sin\left(\omega_{\text{res}}(t - t_{01})\right) \\ & + \left(i_{\text{res\_sec}}(t_{01}) - i_{L1}(t_{01})\right) \cdot \cos\left(\omega_{\text{res}}(t - t_{01})\right) \\ & + \frac{V_s - V_o}{L_{\text{res\_sec}} + L1}(t - t_{01}) \end{aligned} \tag{11}$$

$$\begin{aligned} v_{C\text{res}}(t) = {} & -\left(\frac{L_{\text{res\_sec}} \cdot V_o + L1 \cdot V_s}{L_{\text{res\_sec}} + L1}\right) \cdot \cos\left(\omega_{\text{res}}(t - t_{01})\right) \\ & + \frac{i_{\text{res\_sec}}(t_{01}) - i_{L1}(t_{01})}{C_{\text{res}}\omega_{\text{res}}} \cdot \sin\left(\omega_{\text{res}}(t - t_{01})\right) \\ & + \frac{L_{\text{res\_sec}} \cdot V_o + L1 \cdot V_s}{L_{\text{res\_sec}} + L1}. \end{aligned} \tag{12}$$

At $t = t_{01}$, the term $i_{\text{res\_sec}}(t_{01}) - i_{L1}(t_{01}) = 0$ in (10) and (11). Now, we can discover the impacts of all the information of design parameters in $i_{\text{res\_sec}}$ and $v_{C\text{res}}$. For example, $i_{\text{res\_sec}}$ is a linear function plus a sine function and the peak of $i_{\text{res\_sec}}$ is a function of V_s, V_o, and the tank elements. For the function of $v_{C\text{res}}$, the peak will be $2 \times \frac{L_{\text{res\_sec}} \cdot V_o + L1 \cdot V_s}{L_{\text{res\_sec}} + L1}$ and it is worth noting that the peak value of $v_{C\text{res}}$ is not a function of C_{res} after all

$$\begin{aligned} i_{L1}(t) = {} & i_{\text{res\_sec}}(t) - \left(C_{\text{res}}\left(\frac{L_{\text{res\_sec}} \cdot V_o + L1 \cdot V_s}{L_{\text{res\_sec}} + L1}\right) \cdot \omega_{\text{res}}\right) \\ & \cdot \sin\left(\omega_{\text{res}}(t - t_{01})\right) + \left(i_{\text{res\_sec}}(t_{01}) - i_{L1}(t_{01})\right) \\ & \cdot \cos\left(\omega_{\text{res}}(t - t_{01})\right). \end{aligned} \tag{13}$$

If the output load is heavy, after on time t_{shift} expires and $v_{C\text{res}}$ is not reaching zero yet, then Mode 3 (bleeding mode) exists. And the bleeding mode ends when $v_{C\text{res}}$ discharges to zero. Tank current $i_{\text{res\_sec}}$ and voltage $v_{C\text{res}}$ can be calculated in

$$\begin{aligned} i_{\text{res\_sec}}(t) = {} & \left(\frac{i_{L1}(t_2) - i_{\text{res\_sec}}(t_2)}{L_{\text{res\_sec}} + L1}\right) \cdot L1 \cdot \cos\left(\omega_{\text{res}}(t - t_2)\right) \\ & + \frac{\frac{V_o}{L_{\text{res\_sec}} + L1} - \frac{v_{C\text{res}}(t_2)}{L_{\text{res\_sec}}}}{\omega_{\text{res}}} \cdot \sin\left(\omega_{\text{res}}(t - t_2)\right) \\ & - \frac{V_o}{L_{\text{res\_sec}} + L1}(t - t_2) + i_{L1}(t_2) \\ & - \frac{i_{L1}(t_2) - i_{\text{res\_sec}}(t_2)}{L_{\text{res\_sec}} + L1} \cdot L1 \end{aligned} \tag{14}$$

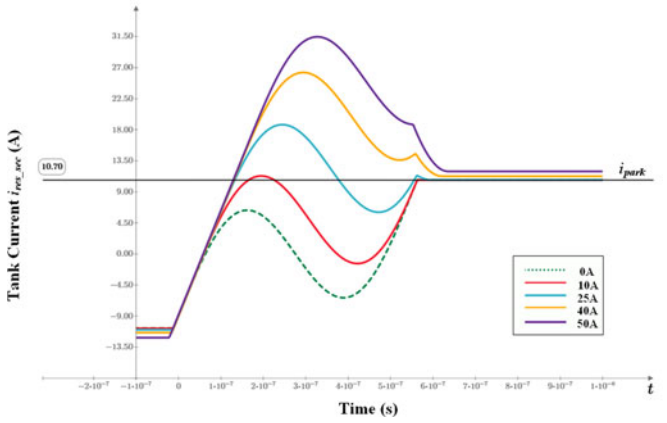

Fig. 17. Modeled tank current $i_{\text{res\_sec}}$ at different output current conditions and $V_{\text{in}} = 54\,\text{V}$.

$$\begin{aligned} v_{C\text{res}}(t) = {} & \frac{i_{L1}(t_2) - i_{\text{res\_sec}}(t_2)}{C_{\text{res}}\omega_{\text{res}}} \cdot \sin\left(\omega_{\text{res}}(t - t_2)\right) \\ & + \left(v_{C\text{res}}(t_2) - \frac{L_{\text{res\_sec}} \cdot V_o}{L_{\text{res\_sec}} + L1}\right) \cdot \cos\left(\omega_{\text{res}}(t - t_2)\right) \\ & + \frac{L_{\text{res\_sec}} \cdot V_o}{L_{\text{res\_sec}} + L1}. \end{aligned} \tag{15}$$

The output inductor current can be also derived as follows:

$$\begin{aligned} i_{L1}(t) = {} & i_{\text{res\_sec}}(t) - \left(i_{\text{res\_sec}}(t_2) - i_{L1}(t_2)\right) \\ & \cdot \cos\left(\omega_{\text{res}}(t - t_2)\right) - \left(C_{\text{res}}\left(v_{C\text{res}}(t_2)\right.\right. \\ & \left.\left. - \frac{L_{\text{res\_sec}} \cdot V_o}{L_{\text{res\_sec}} + L1}\right) \cdot \omega_{\text{res}}\right) \cdot \sin\left(\omega_{\text{res}}(t - t_2)\right). \end{aligned} \tag{16}$$

In Fig. 10, the time t_3 can be solved from (17) when $v_{C\text{res}}(t)$ decays to zero, where k_a, k_b, and k_c can be found in (18)–(20)

$$k_a \cdot \sin\left(\omega_{\text{res}} \cdot t_3\right) + k_b \cdot \cos\left(\omega_{\text{res}} \cdot t_3\right) + k_c = 0 \tag{17}$$

$$k_a = \frac{i_{L1}(t_2) - i_{\text{res\_sec}}(t_2)}{C_{\text{res}}\omega_{\text{res}}} \tag{18}$$

$$k_b = v_{C\text{res}}(t_2) - \frac{L_{\text{res\_sec}} \cdot V_o}{L_{\text{res\_sec}} + L1} \tag{19}$$

$$k_c = \frac{L_{\text{res\_sec}} \cdot V_o}{L_{\text{res\_sec}} + L1}. \tag{20}$$

The time t_3 then can be solved using (21) for different k_a conditions

$$t_3 = \begin{cases} \dfrac{\arcsin\left(\frac{k_c}{\sqrt{k_a{}^2 + k_b{}^2}}\right) - \arctan\left(\frac{k_b}{k_a}\right)}{\omega_{\text{res}}} + t_2, & k_a < 0 \\ \dfrac{\arcsin\left(\frac{k_c}{\sqrt{k_a{}^2 + k_b{}^2}}\right) - \arctan\left(\frac{k_b}{k_a}\right) + \pi}{\omega_{\text{res}}} + t_2, & k_a \geq 0 \end{cases}. \tag{21}$$

Finally, the tank current $i_{\text{res\_sec}}$, the resonant capacitor voltage $v_{C\text{res}}$, and the output inductor current i_{L1} are shown in Figs. 17–19.

In Fig. 17, the tank current on the secondary side is modeled and plotted at different operating conditions and $V_{\text{in}} = 54\,\text{V}$.

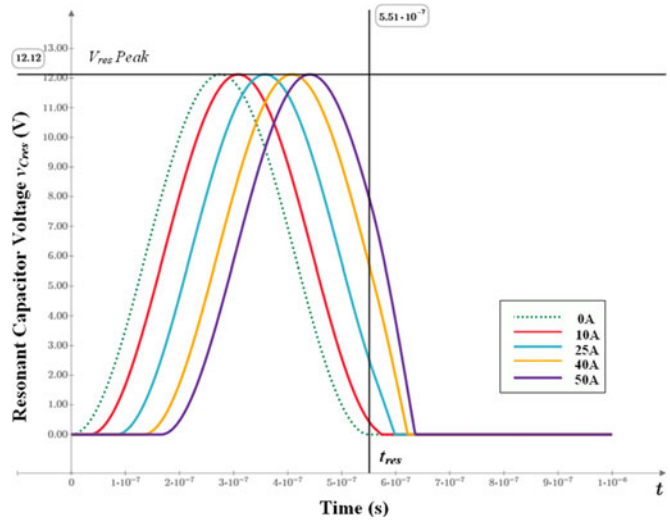

Fig. 18. Modeled resonant capacitor voltage $v_{C\text{res}}$ at different output current conditions and $V_{\text{in}} = 54\,\text{V}$.

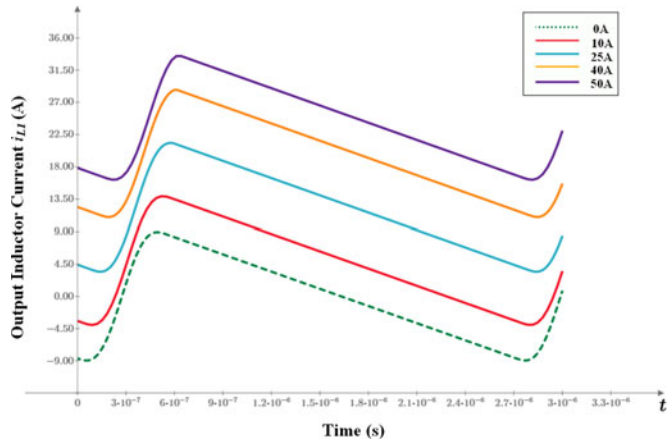

Fig. 19. Modeled output inductor current i_{L1} at different output current conditions and $V_{\text{in}} = 54\,\text{V}$.

From the plots, it reveals the following: 1) the parking current is very similar across full load range to provide ZVS even at light load; and 2) at heavy load, the bleeding mode occurs, where i_{res} starts reducing until t_3. It is worth noting that the load independent i_{park} current level (for switches A and B to achieve ZVS in Fig. 5) is very different from the conventional ZVS-PSFB converter. In conventional ZVS-PSFB converter, this load dependent current level (i_p at time t_0 or t_4 in Fig. 1) is too low at light load to achieve ZVS for switches A and B, but at heavy load this current level becomes too high and introduces more circulating power losses. In the QR-PSFB converter, the i_{park} design parameter can be optimized to provide sufficient energy for ZVS at light load, but avoid unnecessary circulating losses for heavy load. The parking current level and ZVS range for different operating conditions and component tolerances are studied in more details in Section IV-A.

The function of $v_{C\text{res}}(t)$ with different output currents I_o (0–50 A) are plotted in Fig. 18. For $I_o = 0\,\text{A}$, the dotted green curve has resonance with duration of 551 ns and can be calculated using (10). While I_o is increasing, the curve will be shifted toward the left in time, the bleeding mode happens after 551 ns and we can see the capacitor discharging in different rates at different output loading. The higher the output current, the stronger the bleeding mode will be, so that the capacitor voltage $v_{C\text{res}}(t)$ discharges faster to zero. And the average value of $v_{C\text{res}}$ per phase in the current doubler will be the output voltage.

The function of $i_{L1}(t)$ with different output currents I_o (0–50 A) are plotted in Fig. 19. It is worth noting that the waveform is not exactly the same as PWM converters, such as Buck converter (in PWM converter, the inductor current has triangular waveform). And during Mode 2, the resonance is observed as well in the waveform of $i_{L1}(t)$. Also, for PoL application, the inductance is usually small to improve the dynamic response of the converter [12], therefore, the ripple of output inductor current is rather high (∼18 Apk-pk) and cannot be ignored anymore [19].

TABLE I
REFERENCE DESIGN PARAMETER OF THE APPLICATION EXAMPLE

Description	Value
Input voltage, V_{in}	40–60 V, 54 V typical [1]
Output voltage, V_o	1.2 V (+/−10%)
Output current, I_o	25 A
Turns ratio, N_e	7:1
Resonant inductance, L_{res}	2.5 μH (+/−10%)
Resonant capacitance, C_{res}	68 nF ∗ 2 + 33 nF ∗ 2 = 202 nF (+/−5%)
Output inductor, L1 and L2	150 nH (+/−10%)
Output capacitance, C_o	330 μF × 1 (SP-CAP) + 22 μF × 30 (MLCC)
Constant on time, T_{shift}	575 ns
Primary-side FET (FET A, B, C, D)	75 V, 35 A, 30 mΩ
Secondary-side FET (SR1 and SR2)	30 V, 75 A, 1.3 mΩ, 2 in parallel

IV. Design with the Proposed Modeling

To start a new design for 54–1.2 V 25 A VR, transformer turns ratio should be selected to properly step down the primary input voltage to around 6–8 V on the secondary of the transformer. In the initial reference design, the turns ratio is set to 7:1. The targeted switching frequency is 300–400 kHz and t_{shift} will be around 550–650 ns. Due to the fast dynamic response requirement in PoL VR application, the output inductor should be relatively small and 150 nH is a typical design value to start with. In this section, optimization of the design process will be presented. It will demonstrate that for the same resonant frequency and similar switching frequency, the higher L_{res}, the rms current will be reduced in the tank for better efficiency. However, the secondary-side stress will be increased and the output power capability will be reduced. So, L_{res} for this application is selected around 2–4 μH to achieve a good design trade-off and using (1) C_{res} can be calculated. The design example is provided based on the proposed modeling method and the reference design parameter is shown in Table I.

A. Parking Current Level for ZVS

Sufficient parking current level is an important design parameter for QR-PSFB converter to achieve ZVS on the primary

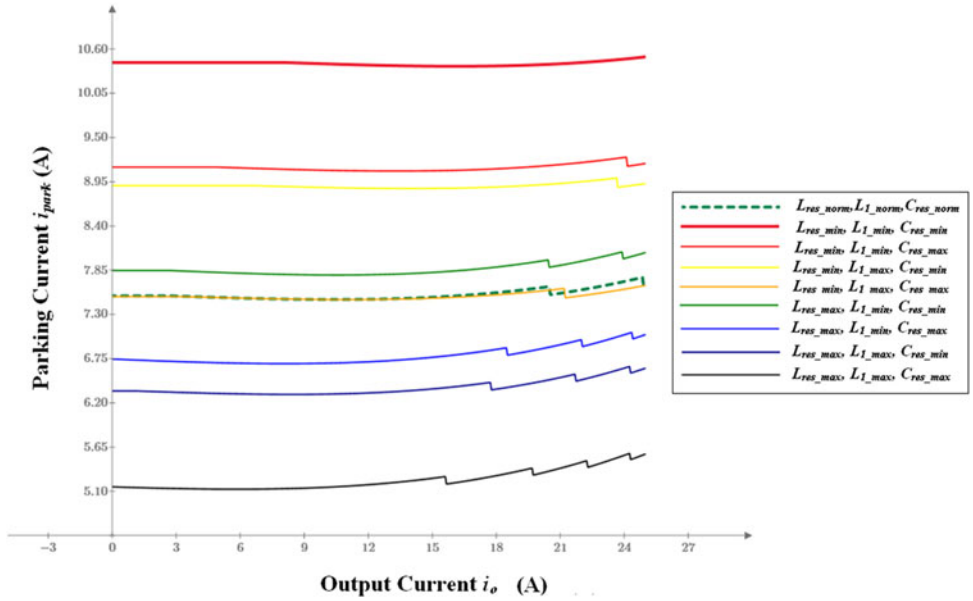

Fig. 20. Modeled parking current at different working conditions and $V_{\text{in}} = 40\,\text{V}$.

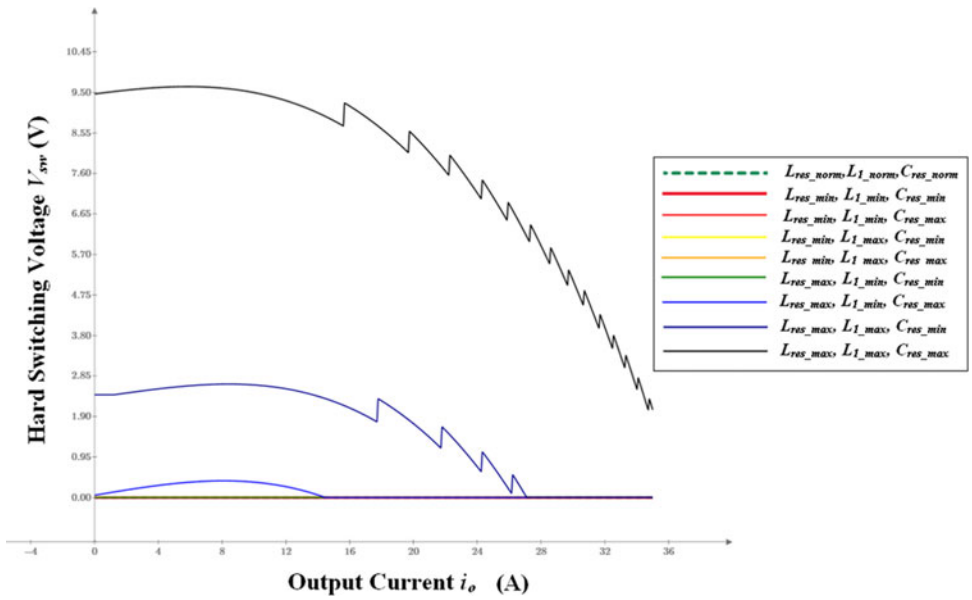

Fig. 21. Modeled hard switching voltage at different working conditions and $V_{\text{in}} = 40\,\text{V}$.

side; however, if the parking current is too high, efficiency will be lower because of high circulating energy. Using the model, we can plot i_{park} for different working conditions. And due to the lower current slew rate during Mode 1 at $V_{\text{in\_min}} = 40\,\text{V}$, we need to make sure we have enough parking current and energy to achieve ZVS. And tolerances of the resonant tank elements are considered as well and plotted in Fig. 20. The following points are worth noting: 1) the lowest parking current occurs when all the elements are at their maximum values, and 2) the parking current is nearly constant across the load range.

And using the parking current information, the switching voltage on the primary side V_{sw} can be estimated in (22), where C_{eq} is the equivalent output capacitance of the MOSFET. If the parking energy is enough to discharge the output capacitance of the primary-side FETs, ZVS turn-on can be achieved and $V_{\text{sw}} = 0$; otherwise, there will be a certain level of hard switching

$$V_{\text{sw}} = \begin{cases} V_{\text{in}} - \sqrt{\frac{L_{\text{res}}}{C_{\text{eq}}}} \cdot I_{\text{park}} & \left(V_{\text{in}} - \sqrt{\frac{L_{\text{res}}}{C_{\text{eq}}}} \cdot I_{\text{park}}\right) > 0 \\ 0 & \left(V_{\text{in}} - \sqrt{\frac{L_{\text{res}}}{C_{\text{eq}}}} \cdot I_{\text{park}}\right) \le 0 \end{cases}. \quad (22)$$

The hard switching voltage level can be plotted in Fig. 21 for different tank parameters considering component tolerance at $V_{\text{in}} = 40\,\text{V}$. In most of the cases, ZVS can be achieved across

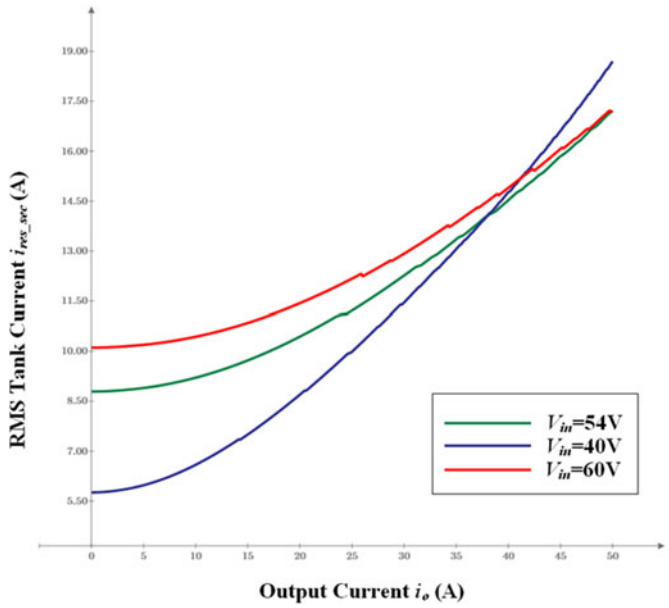

Fig. 22. Root-mean-square value of the secondary-side transformer current.

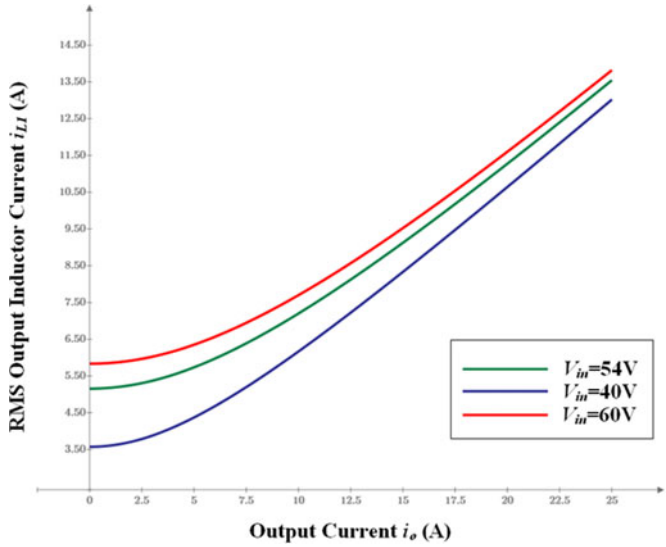

Fig. 23. Root-mean-square value of the output inductor current.

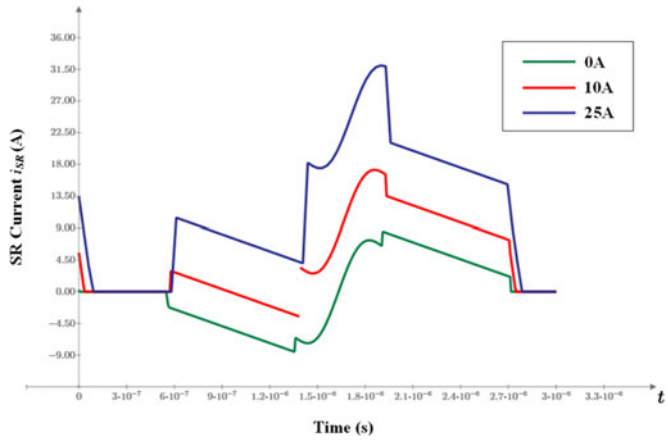

Fig. 24. SR FET current waveform at different operating conditions.

the full load range. The worst case condition occurs when the resonant inductance L_{res}, the capacitance C_{res}, and the output inductance L1 are all at the maximum value. There will be less than 10 V of hard switching and about 20 mW switching loss per FET, which has minor impact on the efficiency, considering this is the absolutely worst case. This means the reference tank design is very robust for ZVS range.

B. Root-Mean-Square Currents and Conduction Losses

Using the model of i_{res} and i_{L1} discussed in Section III-E, the rms value can be calculated by definition. If needed, we can look at the trend of rms current corresponding to any design parameter. In Fig. 22, it shows the rms of the secondary-side current $i_{\text{res\_sec}}$ at different input voltages and output current conditions. Due to the lowest current ripple at 40 V input, the rms current of the transformer is the lowest. It indicates the duty cycle and turns ratio design of the converter is very critical to minimize the rms losses.

Similarly, the output inductor rms current can be also calculated and it shows in Fig. 23 that even when $V_{\text{in}} = 54\,\text{V}$, $I_o = 0\,\text{A}$, we have about 5.76 A of rms current due to the 18 Apk-pk current ripple shown in Fig. 19. And this 5.76 A rms current will be missed in the loss estimation, if we use the second-order modeling proposed in [19].

By using the $i_{\text{res\_sec}}(t)$ and $i_{L1}(t)$ information, the SR current waveform can be obtained in Fig. 24. And the rms value of the SR current can be calculated for loss estimation as well.

C. Switching Frequency

Using the $v_{C\text{res}}$ model information, it is possible to estimate the switching frequency of the converter under steady state. The average value of $v_{C\text{res}}$ minus the DCR drop across the output inductor should be the output voltage V_o. So by calculating the integral value of $v_{C\text{res}}$, that is $\int_{t_{01}}^{t_{01}+t_{\text{res}}} (v_{C\text{res}}) \cdot dt$ for light load and no load, or $\int_{t_{01}}^{t_3} (v_{C\text{res}}) \cdot dt$ for heavy load, f_{sw} can be estimated as $\frac{V_o + \frac{I_o}{2}\text{DCR}}{f(v_{C\text{res}}) \cdot dt}$, which is derived in (23), where DCR is the dc resistance of the output inductor

$$f_{\text{sw}} = \begin{cases} \dfrac{V_o + \frac{I_o}{2} \cdot DCR}{\int_{t_{01}}^{t_{01}+t_{\text{res}}} [v_{C\text{res}}(t)] \cdot dt} & (t_{01} \le \sigma_0) \\ \dfrac{V_o + \frac{I_o}{2} \cdot DCR}{\int_{t_{01}}^{t_3} [v_{C\text{res}}(t)] \cdot dt} & (t_{01} > \sigma_0) \end{cases} \tag{23}$$

This information can be used to select the transformer core material and estimate core loss, FET turn off losses, gate drive losses, etc. Also, in industrial application, f_{sw} is also very important to design front-end EMI filter corner frequency.

D. Transformer Core Loss Estimation

Transformer core loss can be estimated using Steinmetz's equation [33], the k, α and β parameters can be estimated from the core material datasheet. And the flux density at different load

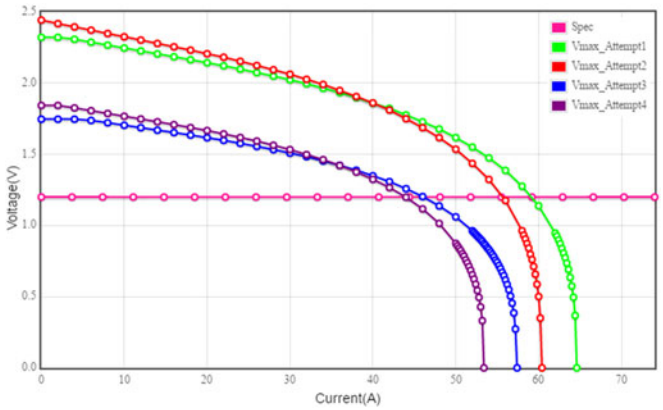

Fig. 25. Output power capability curve in different design conditions.

conditions can be calculated by (24), where A_e is the equivalent core cross section area and N_p is the number of primary-side turns. Eventually, the core loss can be estimated in (25), where V_e is the equivalent core volume

$$B = \begin{cases} \dfrac{N_e \cdot \int_{t01}^{t01+t_{\rm res}} v_{C\rm res}(t)\cdot dt}{2\cdot N_p \cdot A_e} & (t_{01} \le \sigma_0) \\ \dfrac{N_e \cdot \int_{t01}^{t3} v_{C\rm res}(t)\cdot dt}{2\cdot N_p \cdot A_e} & (t_{01} > \sigma_0) \end{cases} \tag{24}$$

$$P_{\rm core} = V_e \cdot k \cdot f^{\alpha} \cdot B^{\beta}. \tag{25}$$

E. Switching Losses

Even through the primary-side FETs are under ZVS turn-on, due to the Miller plateau, the complementary FETs in each of the legs will have turn off losses. We can estimate the turn-off losses in (26), where $t_{\rm off}$ is the turn-off time [29]

$$P_{\rm sw} = \frac{1}{2}\frac{i_{\rm park} \cdot V_{\rm in} \cdot t_{\rm off} \cdot f_{\rm sw}}{N_e}. \tag{26}$$

The gate drive loss can be estimated in (27), where V_g is the gate voltage and Q_g is the total gate charge [29]

$$P_{\rm gate} = V_g \cdot Q_g \cdot f_{\rm sw}. \tag{27}$$

F. Output Power Capability

Due to the unique behavior of secondary-side driver, the converter will have the bleeding mode for a heavy load. Before $v_{C\rm res}$ is fully discharged, we cannot turn on SR on the secondary side or start the next power delivery mode, otherwise, the converter will be damaged. And the main digital controller will prevent this behavior from happening. Based on this limitation, the output voltage and the power capability can be estimated. When $V_{\rm in} = 40$ V, $L_{\rm res}$, $C_{\rm res}$, and the output inductor L1 or L2 are at the maximum value, we will have the lowest output power capability. Theoretically, this reference design tank can deliver up to 55 A output current, considering the worst case tank value, shown in (28), where the function $v_{C\rm res}(V_{\rm max}, t)$ is the resonant capacitor voltage of the tank at the maximum output voltage. Computer program can be used to solve $V_{\rm max}$ and plot the V–I curve in Fig. 25

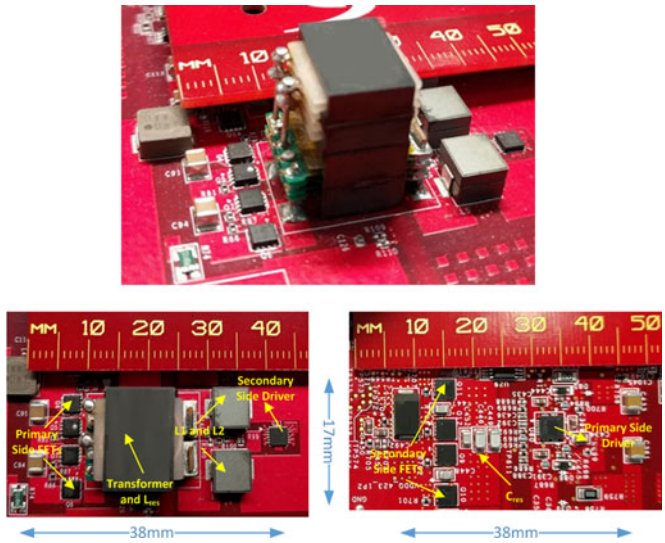

Fig. 26. 54–1.2 V 25 A prototype.

TABLE II
OUTPUT CAPABILITY WITH DIFFERENT DESIGN PARAMETERS

Attempt #	$V_{\rm in}$ (V)	N_e	$L_{\rm res}$ (μH)	$C_{\rm res}$ (nF)	L1 (nH)	I_{o_max} @1.2 V (A)
1	40	7:1	2.5	202	150	59.2
2	40	7:1	2.75	212	165	55.5
3	40	9:1	3.6	202	150	46
4	40	9:1	3.96	212	165	44

$$V_{\rm max} = \begin{cases} \dfrac{\int_{t01}^{t01+t_{\rm res}} v_{C\rm res}(V_{\rm max},t)\cdot dt}{2\cdot t_{\rm shift}} & (t_{01} \le \sigma_0) \\ \dfrac{\int_{t01}^{t3} v_{C\rm res}(V_{\rm max},t)\cdot dt}{2\cdot(\sigma_H + t_3)} & (t_{01} > \sigma_0) \end{cases}. \tag{28}$$

To compare with the reference design, another tank parameter is also plotted with worst tolerance case for output capability. It is worth noting that when the turns ratio N_e increases, the output capability will be reduced. However, later we will see that when N_e is higher, the converter is more efficient, because of the reduced rms conduction losses on the primary side, so there is a design tradeoff to make when selecting proper N_e for design optimization.

V. SIMULATION AND EXPERIMENTAL VERIFICATION

Design prototype is built based on the modeling and design guideline proposed in this paper, shown in Fig. 26.

The access to secondary-side tank current in experiments is very limited, due to the added measurement loop will change the tank characteristics, especially the output inductance. In the experiments, only primary-side current $i_{\rm res\_prim}$ and $v_{C\rm res}$ are measured and shown for the tank information.

TABLE III
COMPARISON OF MODELING, SIMULATION, AND EXPERIMENT AT $I_o = 0$ A

$I_o = 0$ A	i_{park} (A)	i_{res_sec} peak (A)	V_{Cres} peak(V)	f_{sw} (kHz)
Model in [19]	–4.6	11.2	15.4	251
Proposed model	10.7	6.3	12.1	368
Simulation	11	6.5	11.8	377
Experiment	9.6	7.2	12.2	355

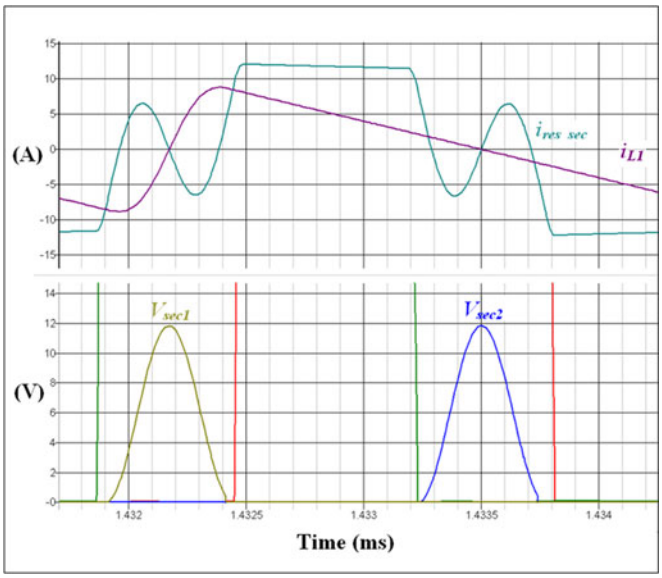

Fig. 27. Simulated results: i_{res_sec} peak = 6.5 A, i_{park} = 11 A, f_{sw} = 377 kHz, at $I_o = 0$ A.

A. Comparison of Modeling, Simulation, and Experiment

1) Comparison at $I_o = 0$ A: Comparisons are made between the model in [19], the proposed model, simulation, and the experimental results for $I_o = 0$ A. The summary is listed in Table III. Simulation results and experiments are shown in Figs. 27 and 28. It demonstrates that the proposed model closely matches the simulation and experiments and the result accuracy is improved significantly compared with the model in [19]. And the model in [19] cannot provide i_{park}, tank voltage V_{Cres} and current i_{res_sec} and switching frequency f_{sw} values correctly; therefore, it cannot be used for guiding the design of this converter.

2) Comparison at $I_o = 10$ A: Comparisons are made between the model in [19], the proposed model, simulation, and the experimental results for $I_o = 10$ A. The summary is listed in Table IV. Simulation results and experiments are shown in Figs. 29 and 30. It demonstrates that the proposed model closely matches the simulation and experiments and the result accuracy is improved significantly compared with the model in [19]. And the model in [19] cannot provide i_{park}, the tank voltage V_{Cres} and current i_{res_sec}, and the switching frequency f_{sw} values correctly; therefore, it cannot be used for guiding the design of this converter.

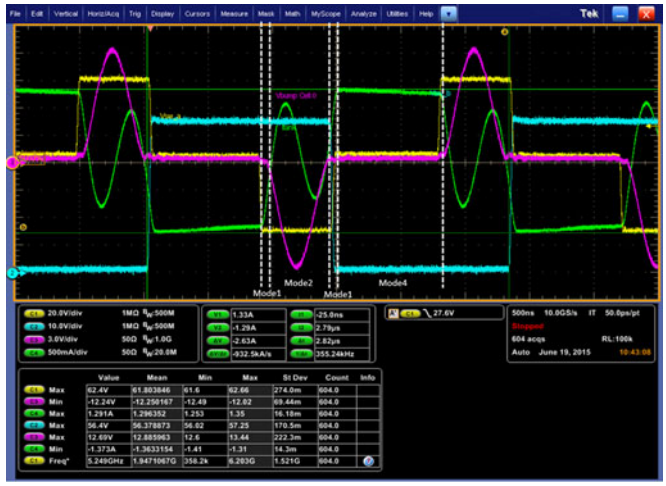

Fig. 28. Experimental results: CH1-Yellow: V_p; CH2-Blue: V_{ds} of FET D; CH3-Pink: V_{p_sec}; CH4-Green: $-i_{res\_prim}$; i_{res_prim} peak = 1.03 A, reflected i_{res_sec} peak = 7.2 A, i_{park} = 9.6 A, f_{sw} = 355 kHz, at $I_o = 0$ A.

TABLE IV
COMPARISON OF MODELING, SIMULATION, AND EXPERIMENT AT $I_o = 10$ A

$I_o = 10$ A	i_{park} (A)	i_{res_sec} peak (A)	V_{Cres} peak(V)	f_{sw} (kHz)
Model in [19]	–4.4	16.1	15.4	253
Proposed model	10.7	11.4	12.1	370
Simulation	11.4	11.4	11.8	380
Experiment	10.5	11.2	11.6	370

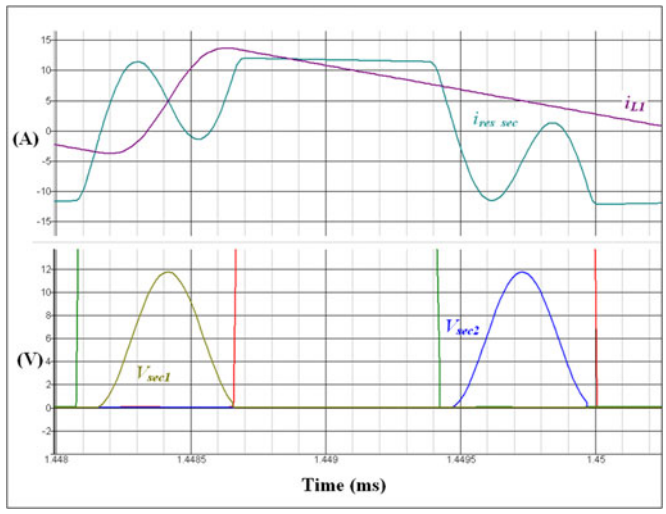

Fig. 29. Simulated results: i_{res_sec} peak = 11.4 A, i_{park} = 11.4 A, f_{sw} = 380 kHz, $I_o = 10$ A.

3) Comparison at $I_o = 25$ A: Comparisons are made between the model in [19], the proposed model, simulation, and the experimental results for $I_o = 25$ A. The summary is listed in Table V. Simulation results and experiments are shown in Figs. 31 and 32. It demonstrates that the proposed model closely matches the simulation and experiments and the result accuracy is improved significantly compared with the model in [19]. And

Fig. 30. Experimental results: CH1-Yellow: V_p; CH2-Blue: V_{ds} of FET D; CH3-Pink: $V_{\text{p\_sec}}$; CH4-Green: $-i_{\text{res\_prim}}$; $i_{\text{res\_prim}}$ peak = 1.6 A, reflected $i_{\text{res\_sec}}$ peak = 11.2 A, i_{park} = 10.5 A, f_{sw} = 370 kHz, I_o = 10 A.

Fig. 32. Experimental results: CH1-Yellow: V_p; CH2-Blue: V_{ds} of FET D; CH3-Pink: $V_{\text{p\_sec}}$; CH4-Green: $-i_{\text{res\_prim}}$; $i_{\text{res\_prim}}$ peak = 2.54 A, reflected $i_{\text{res\_sec}}$ peak = 17.8 A, i_{park} = 10.5 A, f_{sw} = 386 kHz, I_o = 25 A.

TABLE V
COMPARISON OF MODELING, SIMULATION, AND EXPERIMENT AT I_o = 25 A

I_o = 25 A	i_{park} (A)	$i_{\text{res\_sec}}$ peak (A)	$V_{C\text{res}}$ peak (V)	f_{sw} (kHz)
Model in [19]	–4.1	23.8	15.4	257
Proposed model	10.7	18.8	12.1	374
Simulation	11.5	18.9	11.8	386
Experiment	10.5	17.8	11.1	386

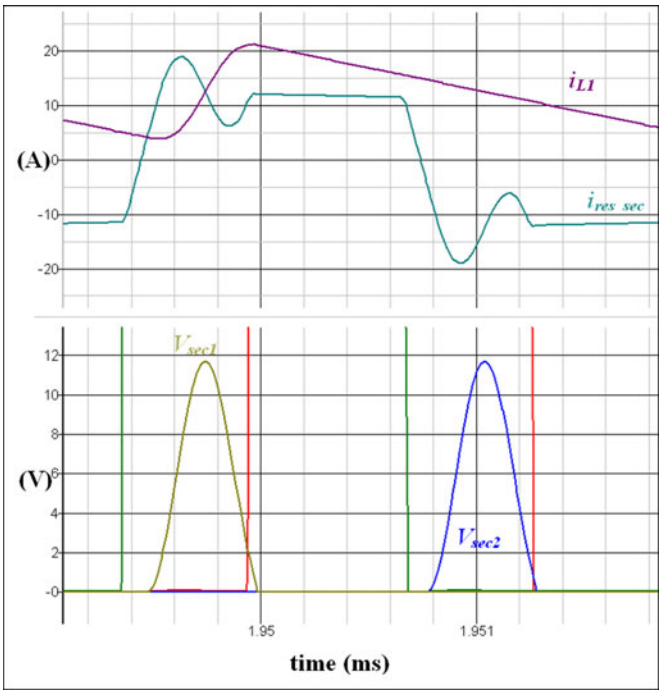

Fig. 31. Simulated results: $i_{\text{res\_sec}}$ peak = 18.9 A, i_{park} = 11.5 A, f_{sw} = 386 kHz, I_o = 10 A.

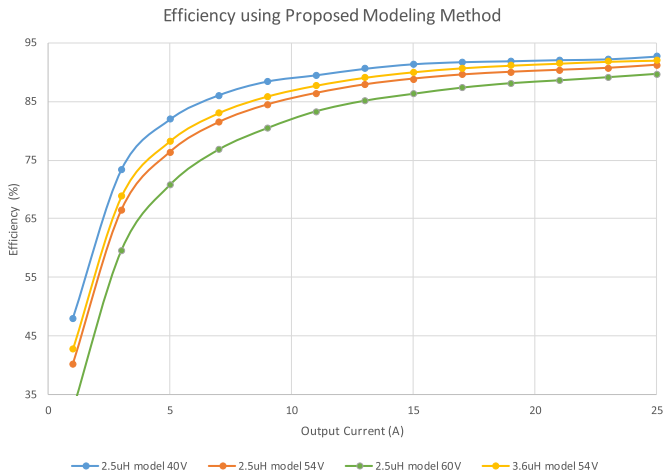

Fig. 33. Efficiency curves using the proposed model at different design conditions.

the model in [19] cannot provide i_{park}, the tank voltage $V_{C\text{res}}$ and current $i_{\text{res\_sec}}$, and the switching frequency f_{sw} values correctly; therefore, it cannot be used for guiding the design of this converter.

B. Efficiency and Losses

Finally, we have all the information to estimate the efficiency of the design. Modeled efficiency curves are shown in Fig. 33 for the reference design in Table I at different input voltages.

It is worth noting that at lower input voltages, the efficiency is higher, which indicates a way of optimizing the efficiency of QR-PSFB converter by increasing the effective duty ratio. Therefore, the improved design proposes a higher turns ratio (N_e = 9) but at the same time attempts to maintain similar equivalent resonant tank design (L_{res} = 3.6 μH) seen on the secondary side. And at 25 A full load, the improved design offers 1% higher efficiency and more than 10% loss reduction.

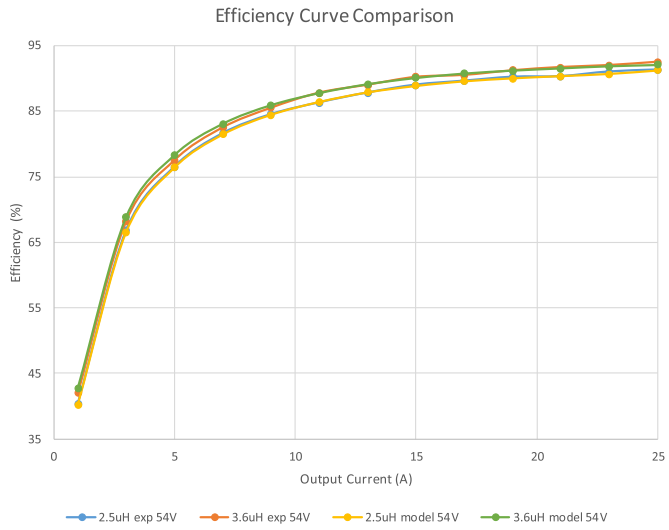

Fig. 34. Efficiency comparison between experimental results and proposed model.

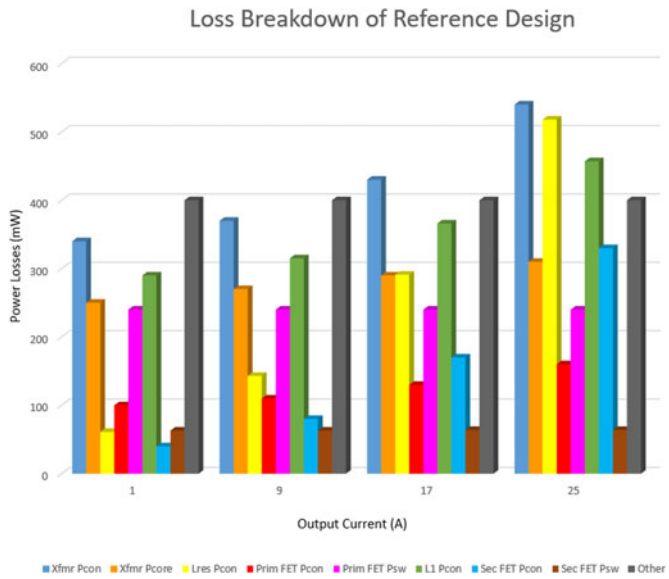

Fig. 35. Loss breakdown of the reference design.

However, we can observe from the Fig. 25 that when N_e is higher, the output capability is lower.

Efficiency is measured and compared on the porotype with the reference design and the improved design in Fig. 34. The modeled efficiency matches the measured result very well in both of the design cases. And the error is less than 0.2% across the load range.

The modeled power loss breakdown is shown in Fig. 35. We can observe that the conduction losses of the transformer and the FETs are the dominant losses, especially at heavy-load condition. The "Other" losses are mainly the bias power of the main digital controller.

The modeled power loss breakdown is shown for the improved design in Fig. 36. The major loss saving is from the conduction losses of the transformer, resonant inductor L_{res} and primary FETs.

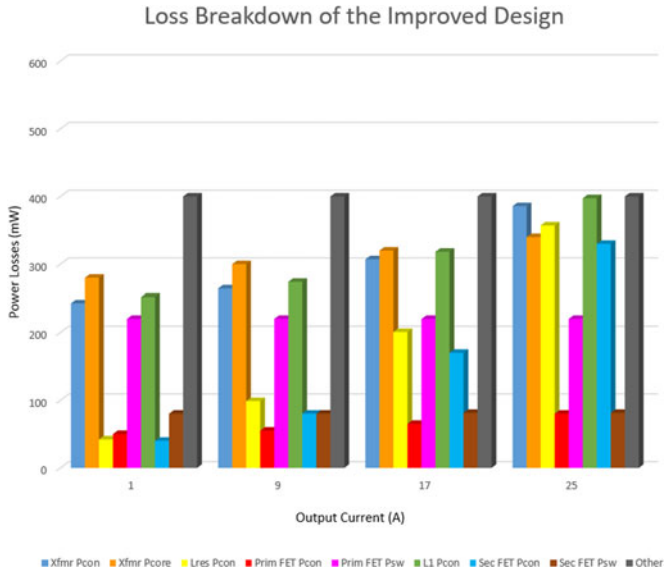

Fig. 36. Loss breakdown of the improved design ($N_e = 9:1$, $L_{\text{res}} = 3.6\,\mu$H).

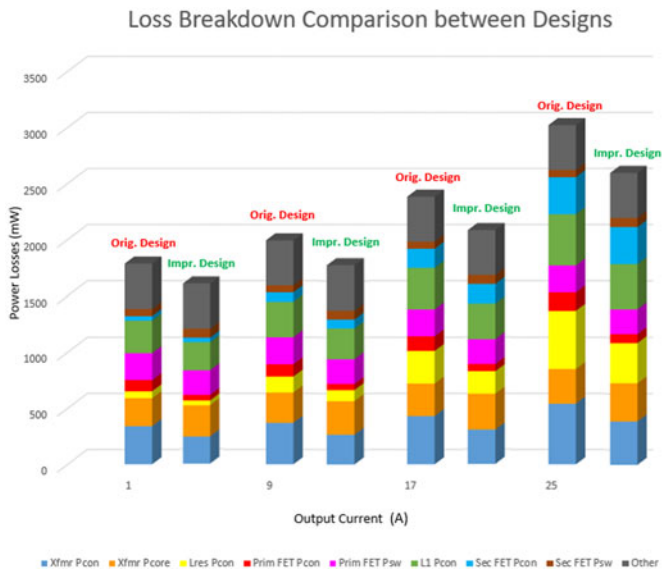

Fig. 37. Loss breakdown comparison between the original reference design and the improved design.

The loss breakdown comparison between the reference design and the improved design is shown in Fig. 37. And transformer conduction loss, resonant inductor conduction loss, and FET conduction loss are, respectively, reduced in the improved design, mainly due to the rms current reduction. At minimum load, the improved design reduces total power losses by more than 170 mW. While at maximum load, the improved design reduces total power losses by more than 420 mW.

C. Transient Performance

Due to the QR behavior of the resonant inductor L_{res} and capacitor C_{res} (a zero-order capacitor with no dynamics [39],

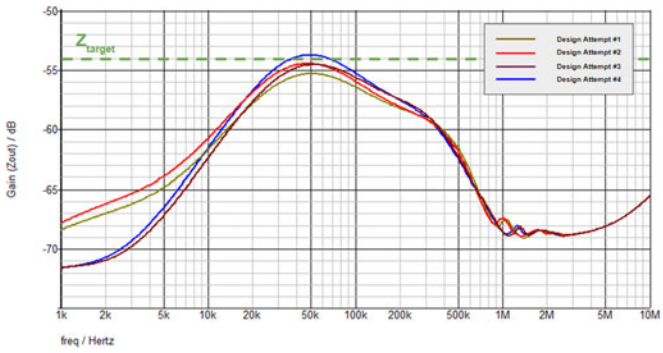

Fig. 38. Closed-loop output impedance comparison with different design attempt parameters.

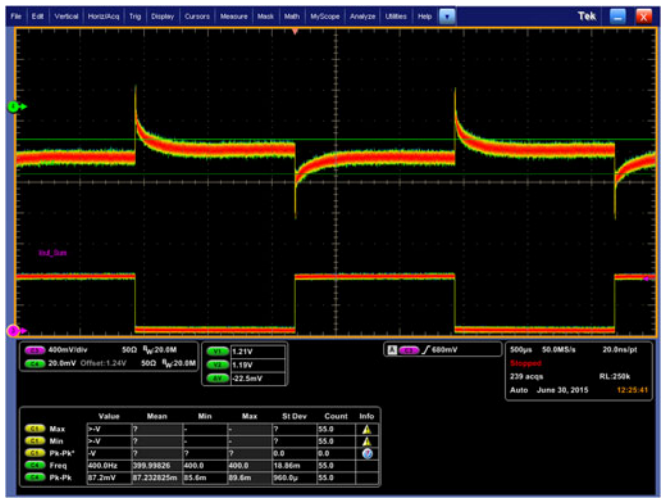

Fig. 39. Load transient performance at 400 Hz switching, 0−25 A, 12.5 A/μs (CH3-Pink: current reporting signal for the load tester, 15 mV/A; CH4-Green: Output Voltage with 20 MHz BW).

because the capacitor voltage is forced to zero periodically), the dynamic response of this converter is very similar to a Buck derived converter. Therefore, a conventional proportional-integral-derivative (PID) controller can be used for output voltage regulation by controlling the switching frequency for the COT control. When the load transient frequency is above the BW of the converter, the converter loop will not help to reduce the closed-loop output impedance of the regulator anymore. Therefore, the decoupling capacitor network or power delivery/distribution network (PDN) design becomes very critical to suppress the output voltage ripples by providing low enough output impedance [11], [34]. In PDN and power integrity design, a target impedance is used to set the goal of the output impedance of the power source in the frequency domain [40]–[42]. And the target impedance can be set based on (29) [40]–[42], where $\Delta V_{\max}$ is the allowable output voltage ripple and $\Delta I_{\text{trans\_max}}$ is the maximum current transient step value. For example, if we choose $\Delta V_{\max} = 50$ mV to leave 10 mV design margin (for 5% of 1.2 V, that is, 60 mV output voltage ripple or 120 mVpk-pk absolute maximum ripple) and $\Delta I_{\text{trans\_max}} = 25$ A, the target impedance will be 2 mΩ (or ~ -54 dBΩ shown with a dashed green line in Fig. 38)

$$Z_{\text{target}} = \frac{\Delta V_{\max}}{\Delta I_{\text{trans\_max}}}. \tag{29}$$

Closed-loop output impedance is simulated with different design attempt parameters listed in Table II, and the result is shown in Fig. 38. To analyze the converter design parameter impact on the closed-loop output impedance, in the simulations, the same PID controller is used ($K_p = 0.5$, $K_i = 5000$, $K_d = 4 \times 10^{-6}$). The system loop crossover frequency is >75 kHz and phase margin is >60° for all design attempts. From the result in Fig. 38, it is worth noting that when the turns ratio N_e is changed from 7:1 (for example, design attempt #1) to 9:1 (for example, design attempt #3), the peak closed-loop output impedance will become higher around 50 kHz, due to the worse loop response caused by the lower reflected secondary-side voltage V_s. With the lower reflected secondary-side voltage V_s in higher transformer turns ratio design attempts, the converter response performance, especially for loading transient (from light to heavy load), will be compromised, because of the following: 1) the rising slew rate of the output inductor current is decreased; and 2) the steady state duty cycle is closer to the maximum, resulting in limited headroom to further boost the duty cycle. The output inductor impact on the transient performance of QR-PSFB is very similar to the conventional Buck converter. When the output inductor is higher, the transient response of the converter will be degraded and the peak closed-loop output impedance will be higher, too.

Therefore, there is a design optimization to make between transient performance and power conversion efficiency. After making the efficiency improvement with higher turns ratio $N_e = 9:1$ and $L_{\text{res}} = 3.6\,\mu$H in Section V-B, from the output impedance simulation in Fig. 38, it shows that it is very marginal to continue the efficiency improvement trend by increasing the turns ratio N_e or L_{res} further, as the closed-loop output impedance is getting closer to Z_{target}. However, with the turns ratio $N_e = 9:1$ and $L_{\text{res}} = 3.6\,\mu$H (in design attempt #3), Z_{target} can still be met with one 330 μF SP-CAP [43] (Specialty Polymer Aluminum capacitor, self-resonant frequency is ~400 kHz) and thirty 22 μF MLCCs (multilayer ceramic capacitors, self-resonant frequency is ~2 MHz). Further suppression on the output impedance can be made by adding more SP-CAPs, but the solution size and cost will be increased.

The transient performance of the prototype is tested with high rate current transient ($di/dt > 10$ A/μs) at different load switching frequencies. And the scope is set to fast acquisition, so that we can see multiple transient events. The load tester will report the transient current in a voltage signal with the gain of 15 mV/A and 0% to 100% of $I_{\text{o\_max}}$ is used for load step.

The transient performance of the prototype is tested at 400 Hz load switching to show the loop response of the converter in Fig. 39. The output variation is ~87 mVpk-pk.

The transient performance of the prototype is tested at 100 kHz load switching to show the loop response of the converter and this frequency is just over the bandwidth of the

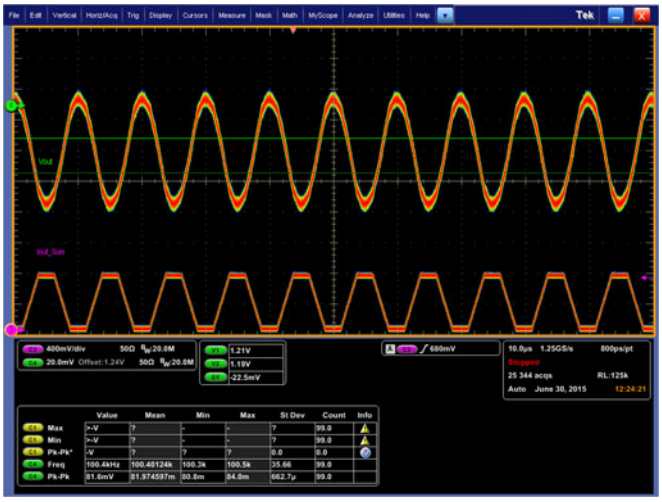

Fig. 40. Load transient performance at 100 kHz switching, 0−25 A, 12.5 A/μs (CH3-Pink: current reporting signal for the load tester, 15 mV/A; CH4-Green: output voltage with 20 MHz BW).

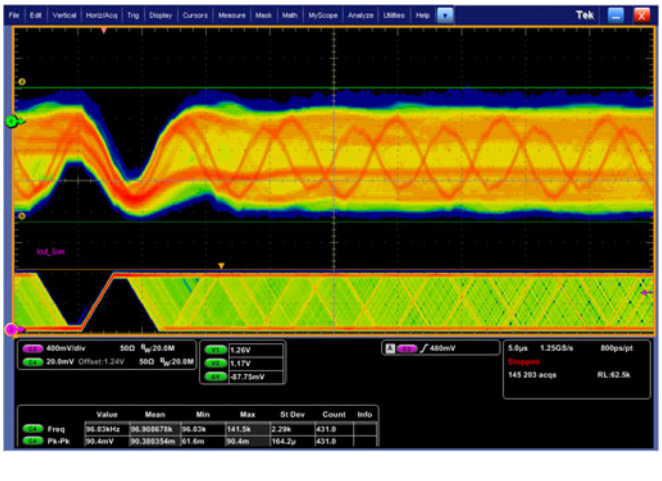

Fig. 41. Load transient performance with frequency sweeping from 100 Hz to 200 kHz, 0−25 A, 12.5 A/μs (CH3-Pink: current reporting signal for the load tester, 15 mV/A; CH4-Green: output voltage with 20 MHz BW).

converter. The result shows in Fig. 40 that at 100 kHz, the PDN design is sufficient to meet the target output impedance. The output variation is ∼82 mVpk-pk. Load transient with frequency sweeping for a wide range of the PDN validation is shown next.

To scan the full closed-loop output impedance using different switching load [11], [34], the scope is set to fast acquisition + infinite persistence mode in Fig. 41. We can measure the worst-case output voltage variation is 90.4 mVpk-pk across the frequency range of 100 Hz to 200 kHz, which meets the ±5% of 1.2 V (120 mVpk-pk absolute maximum ripple) requirement and leaves ∼25% performance margin. This matches the simulation result in Fig. 38 very well, where the peak closed-loop output impedance is −54.5 dB (equivalent to 92 mVpk-pk output voltage ripple).

VI. Conclusion

In this paper, a new modeling technique for a QR-PSFB converter is presented. In Section I, power architecture for 54 V-PoL using two-stage conversion is reviewed. And the conventional PSFB is reviewed and the issues of this topology are highlighted. In Section II, the QR-PSFB with COT control is presented under light and heavy-load conditions and this section provides the fundamental for the modeling. Equivalent circuit and state equation are studied for each of the modes in QR-PSFB converter in Section III and tank current and voltage information is solved for different operating conditions. Design guidelines are provided for a 54–1.2 V 25 A reference design in Section IV, including the ZVS range, power losses, power capability, and component tolerances. Design improvement is made based on the modeling results and guidance. Simulation and experimental results are provided to verify the modeling technique in a 54–1.2 V 25 A dc–dc converter design and confirm the accuracy of the proposed modeling method.

References

[1] Open Compute Project (OCP), *Open Rack Standard V2.0*. Jan. 2017. [Online]. Available: http://files.opencompute.org/oc/public.php?service=files&t=1088a8d608fb48fd46828af3fdf9a861

[2] L. A. Barroso and U. Hölzle, "The case for energy-proportional computing," *IEEE Comput.*, vol. 40, pp. 33–37, Dec. 2007.

[3] L. A. Barroso, J. Clidaras, and U. Hölzle, "The datacenter as a computer: An introduction to the design of warehouse-scale machines," Second Edition, Morgan & Claypool Publishers: USA, 2013.

[4] Delta Electronics, Inc., 600W Quarter Brick, DS_Q54SG12050. Sep. 2016. [Online]. Available: at:http://www.deltaww.com/filecenter/Products/download/01/0102/datasheet/DS_Q54SG12050.pdf

[5] GE, QBDE067A0B, *Barracuda*^{TM} *Series DC-DC Power Modules*. Sep. 2016. [Online]. Available: http://apps.geindustrial.com/publibrary/checkout/QBDE067A0B?TNR=Data%20Sheets%7CQBDE067A0B%7CPDF&filename=QBDE067A0B.pdf

[6] Ericsson, BMR458 Series, *Digital 1/4 Brick 650W, BMR458 0011/002*. Jun. 2016. [Online]. Available: https://www.ericsson.com/ourportfolio/products/

[7] P. Yeaman, "High current, low voltage solution for microprocessor applications from 48V input," in *Proc. Power Convers. Intell. Motion Eur.*, May 2007, pp. 1–6.

[8] P. Yeaman and E. Oliveira, "A high efficiency high density voltage regulator design providing VR 12.0 compliant power to a microprocessor directly from a 48V input," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2013, vol. 13, pp. 410–414.

[9] Y. Ren, M. Xu, J. Sun, and F. C. Lee, "A family of high power density unregulated bus converters," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1045–1054, Sep. 2005.

[10] W. Huang, G. Schuellein, and D. Clavette, "A scalable multiphase buck converter with average current share bus,"in *Proc. 18th Annu. IEEE Appl. Power Electron. Conf. Expo. 2003*, Miami Beach, FL, USA, vol. 1, 2003, pp. 438–443.

[11] K. Yao *et al.*, "Adaptive voltage position design for voltage regulators," in *Proc. 19th Annu. Appl. Power Electron. Conf. Expo. 2004*, 2004, vol. 1, pp. 272–278.

[12] P.-L. Wong, F. C. Lee, P. Xu, and K. Yao, "Critical inductance in voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 485–492, Jul. 2002.

[13] L. Jia and Y.-F. Liu, "Voltage based charge balance controller suitable for both digital and analog implementations," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 930–944, Feb. 2013.

[14] Y. Qiu, J. Sun, M. Xu, K. Lee, and F. C. Lee, "Bandwidth improvements for peak-current controlled voltage regulators," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1253–1260, Jul. 2007.

[15] J. Sun, Y. Qiu, M. Xu, and F. C. Lee, "High-frequency dynamic current sharing analyses for multiphase buck VRs," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2424–2431, Nov. 2007.
[16] M. Xu, J. Zhou, K. Yao, and F. C. Lee, "Small signal modeling of a high bandwidth voltage regulator using coupled inductors," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 399–406, Mar. 2007.
[17] L. Jia, Google Defensive Publication, "Adaptive voltage conversion for energy efficient computing," *Tech. Disclosure Commons*, Jun. 03, 2016. [Online]. Available: http://www.tdcommons.org/dpubs_series/203
[18] M. Ye, M. Xu, and F. C. Lee, "1 MHz multi-resonant push-pull 48 V VRM,"in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2003, vol. 1, pp. 413–419.
[19] L. Huber, K. Hsu, M. M. Jovanovic, D. J. Solley, G. Gurov, and R. M. Porter, "1.8-MHz, 48-V resonant VRM: Analysis, resign, and performance evaluation," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 79–88, Jan. 2006.
[20] Y. Zhang, D. Xu, M. Chen, Y. Han, and Z. Du, "LLC resonant converter for 48 V to 0.9 V VRM,"in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, vol. 3, pp. 1848–1854.
[21] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. Appl. Power Electron. Conf. Expo.*, 2002, vol. 2, pp. 1108–1112.
[22] B. Yang, "Topology investigation of front end DC/DC converter for distributed power system," *Ph.D. dissertation*, Dept. Electr. Comput. Eng., Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2003.
[23] S. De Simone, C. Adragna, C. Spini, and G. Gattavari, "Design-oriented steady-state analysis of LLC resonant converters based on FHA," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom., Motion*, 2006, pp. 200–207.
[24] S. W. Kang, H. J. Kim, and B. H. Cho, "Adaptive voltage-controlled oscillator for improved dynamic performance in LLC resonant converter," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1652–1659, Mar.–Apr. 2016.
[25] Z Hu, Y Liu, and P Sen, "Bang-Bang charge control for LLC resonant converters," *IEEE Trans. Power Electron.*, vol, 30 no. 2, pp 1093–1108, Feb. 2015.
[26] ON semiconductor (formerly Fairchild), FAN7688, Advanced Secondary Side LLC Resonant Converter Controller with Synchronous Rectifier Control. Nov. 2015. [Online]. Available: https://www.fairchildsemi.com/products/power-management/offline-isolated-dc-dc/llc-resonant-and-asymmetric-half-br-idg/FAN7688.html
[27] NXP semiconductor, TEA19161T, Digital Controller for High-Efficiency Resonant Power Supply. Mar. 2016. [Online]. Available: http://www.nxp.com/documents/data_sheet/TEA19161T.pdf?fasp=1&WT_TYPE=Data%20Sheets&WT_VENDOR=FREESCALE&WT_FILE_FORMAT=pdf&WT_ASSET=Documentation&fileExt=.pdf
[28] SLUU109B, Texas Instruments, User's Guide, "Using the UCC3895 in a direct control driven synchronous rectifier applications," Feb. 2009. [Online]. Available: http://www.ti.com/lit/ug/sluu109b/sluu109b.pdf
[29] Sam Abdel-Rahman, Infineon, Design Note DN 2013-01, "Design of phase shifted Full-Bridge converter with current doubler rectifier," Mar. 2013. [Online]. Available: http://www.mouser.com/pdfdocs/2-12.pdf
[30] Texas Instruments, UCC28950 datasheet, "UCC28950 green phase-shifted Full-Bridge controller with synchronous rectification," Mar. 2010. [Online]. Available: http://www.ti.com/lit/ds/symlink/ucc28950.pdf
[31] ST Micro, AN2626, "MOSFET body diode recovery mechanism in a phase-shifted ZVS full bridge DC/DC converter," Sep. 2007. [Online]. Available: http://www.st.com/content/ccc/resource/technical/document/application_note/b9/5e/9f/53/30/d8/49/4d/CD00171347.pdf/files/CD00171347.pdf/jcr:content/translations/en.CD00171347.pdf
[32] S. Shekhawat, M. Rinehimer, and B. Brockway, ON semiconductor (formerly Fairchild), AN7536, "FCS fast body diode MOSFET for phase-shifted ZVS PWM full bridge DC/DC converter," REV. 1.00, Nov. 2005. [Online]. Available: https://www.fairchildsemi.com/application-notes/AN/AN-7536.pdf
[33] Steinmetz's equation, Wikipedia. 2017. [Online]. Available: https://en.wikipedia.org/wiki/Steinmetz%27s_equation
[34] K. Yao, M. Xu, Y. Meng, and F. C. Lee, "Design considerations for VRM transient response based on the output impedance," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1270–1277, Nov. 2003.
[35] Texas Instruments, "LMG5200 48 V to 1V/40A single stage converter reference design," *Application Notes*, Sep. 2016. [Online]. Available: http://www.ti.com/tool/PMP4497
[36] Maxim Integrated, "Maxim integrated 48 V to core solution," Mar. 2017. [Online]. Available: http://www.edn.com/Home/PrintView?contentItemId=4458098
[37] Efficient Power Conversion, "Single-stage 48 V–1 V DC–DC conversion simplifies power distribution while significantly boosting conversion efficiency," *Application Notes*. [Online]. Available: http://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_48 V-1 V.pdf
[38] CPES, Virginia Tech, *High-Efficiency High-Power-Density 48/1V Sigma Converter Voltage Regulator Module*. [Online]. Available: https://www.cpes.vt.edu/library/viewnugget/680
[39] C. K. Tse, "Zero-order switching networks and their applications to power factor correction in switching converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 44, no. 8, pp. 667–675, Aug. 1997.
[40] E. Bogatin, "The power distribution network," in *Signal and Power Integrity—Simplified, 2nd ed*. Prentice Hall: Boston, USA, Jul. 27, 2009.
[41] L. D. Smith and E. Bogatin, "Engineering the power delivery network," in *Principles of Power Integrity for PDN Design—Simplified*, 1st ed. Prentice Hall: Boston, USA, 2017.
[42] L. D. Smith, R. E. Anderson, D. W. Forehand, T. J. Pelc, and T. Roy, "Power distribution system design methodology and capacitor selection for modern CMOS technology," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 284–291, Aug. 1999.
[43] Specialty Polymer Aluminum Capacitor. 2017. [Online]. Available: https://na.industrial.panasonic.com/products/capacitors/polymer-capacitors/sp-cap-polymer-aluminum

Liang Jia (S'08–M'12) received the B.Eng. degree from the School of Mechanical and Electrical Engineering, Soochow University, Suzhou, China, in 2008, and the Master of Applied Science degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 2011.

Since Jan. 2015, he has been a Power Engineer for Consumer Hardware and dc–dc (48 V-PoL) power technology for Global Datacenter Infrastructure at Google Inc., Mountain View, CA, USA. From 2011 to 2015, he was a Product Design Engineer with Philips Electronics North America, Rosemont, IL, USA. His main responsibility is to develop new-generation high-power LED drivers with digital intelligence and better performance. He has published more than 20 technical papers in IEEE Transactions and conferences and has 15 U.S. and international patents pending and 5 IP defensive publications. His current research interests include efficient power conversion and management, wireless power transfer, power delivery solution for high-performance and super computing, battery management for handheld devices, next-generation 48 V-PoL VRs, LED lighting systems, resonant power conversion, digital control technology, power modeling and simulation, power semiconductor devices, and integrated circuits.

Mr. Jia was the recipient of the National Scholarship of China in 2008, Temasek Foundations (Singapore)-Nanyang Technological University LEaRN Exchange Scholarship in 2008, the Tsung-Dao Lee Chinese Undergraduate Research Endowment in 2006, and about 10 other scholarships and awards during his studies. He was a Technical Section Chair in the IEEE ECCE 2015 and was a Reviewer for the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the IEEE TRANSACTIONS ON INDUSTRIAL INFORMATICS.

Srikanth Lakshmikanthan has been the Technical Power Team Manager in Google Hardware, Google Inc., Mountain View, CA, USA, since 2016. He has been with Google as a Staff Hardware Engineer and leading power design solutions in multiple product areas, including data center and Chrome Hardware since 2006.

Xin Li received the B.S. and M.S. degrees in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2003 and 2005, respectively.

From July 2005 to March 2013, he was a Power Electronic Design Engineer and Design Manager at Schneider Electric, where he was engaged in variable-speed drive and active power filter design. From February 2013 to March 2015, he was with Power Integrations as a Lead Application Engineer. He is currently a Technical Lead Manager at Google Inc., Mountain View, CA, USA, where he leads the team to develop power technologies and solutions for Google data center products.

Yan-Fei Liu (M'94–SM'97–F'13) received the Bachelor and Master's degrees from the Department of Electrical Engineering, Zhejiang University, Zhejiang, China, in 1984 and 1987, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, in 1994.

He was a Technical Advisor with the Advanced Power System Division, Nortel Networks, in Ottawa, Canada, from 1994 to 1999. Since 1999, he has been with Queen's University, where he is currently a Professor with the Department of Electrical and Computer Engineering. He has authored over 200 technical papers in the IEEE Transactions and conferences and holds 20 U.S. patents. His current research interests include digital control technologies for high efficiency, fast dynamic response dc–dc switching converter and ac–dc converter with power factor correction, resonant converters and server power supplies, and LED drivers.

Dr. Liu is as an Editor of the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS OF POWER ELECTRONICS (IEEE JESTPE) since 2013, an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2001, and a Guest Editor-in-Chief for the special issue of Power Supply on Chip of the IEEE TRANSACTIONS ON POWER ELECTRONICS from 2011 to 2013. He was also a Guest Editor for special issues of JESTPE: MINIATURIZATION OF POWER ELECTRONICS SYSTEMS in 2014 and Green Power Supplies in 2016. He was the Co-General Chair of ECCE 2015 held in Montreal, Canada, in September 2015. He will be the General chair of ECCE 2019 to be held in Baltimore, MD, USA. He has been the Chair of the PELS Technical Committee on Control and Modeling Core Technologies since 2013 and the Chair of the PELS Technical Committee on Power Conversion Systems and Components from 2009 to 2012. He is also a Principal Contributor for two IEEE standards. He received Premier's Research Excellence Award in 2000 in Ontario, Canada. He also received the Award of Excellence in Technology in Nortel in 1997